Addendum to the PCI 9054 Data Book, Version 2.1

A.   Affected Silicon Revision

Product	Part Number	Description	Production
PCI 9054	PCI 9054-AC50PI	Released 176-pin PQFP Product	February 2002
PCI 9054	PCI 9054-AC50BI	Released 225-pin PBGA Product	February 2002

B.   Documentation Revision

Document	Version/Revision	Description	Publication Date
PCI 9054 Data Book	v2.1	Data Book	January 2000
PCI 9054 Data Book Addendum	r2.4	Data Book Addendum	March 24, 2006
PCI 9054AC Errata	See www.plxtech.com for latest revision	Errata Documentation	
PCI 9054 Design Notes	See www.plxtech.com for latest revision	Design Note Documentation	
PCI 9054 AB to AC Conversion Document	See www.plxtech.com for latest revision	PCI 9054 Conversion from Silicon Revision AB to AC	

C.   Addendum Documentation Summary

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1. M Mode AC Timing Changes

When the PCI 9054 is operated in M mode, the AC timing for the signals listed in the following table take precedence over the values published in Table 13-8 of the *PCI 9054 Data Book, Version 2.1*.

M Mode Timing Table Changes

Signal (Synchronous Outputs) C_L = 50 pF, V_{CC} = 3.0V, T_a = 85 °C	Clock to Out Worst Case (ns) T_{VALID} (Max) PCI 9054 Revision AC (Data Book Addendum r2.2)	Clock to Out Worst Case (ns) T_{VALID} (Max) PCI 9054 Revision AB (Data Book v2.1)
BDIP#	13.2	10.5
LA[0:31]	10.2	10.0
DMPAF	N/A*	13.0
TEA#	9.3	8.5

** **Note:** The DMPAF signal is an asynchronous signal; therefore, it will be caught on the next clock edge.*

2. Hot Swap Control/Status Register Reset Value Change

The specified reset value of the Board Insertion ENUM# Status Indicator, bit 7 of the Hot Swap Control/Status register (HS_CSR; PCI:4Ah, LOC:18Ah) has changed from the value published on page 11-17 of the *PCI 9054 Data Book, Version 2.1*. The new reset value is listed below.

Register 11-33 (HS_CSR; PCI:4Ah, LOC:18Ah) Hot Swap Control/Status

Bit	Description	Value After Reset PCI 9054 Revision AC (Data Book Addendum r2.2)	Value After Reset PCI 9054 Revision AB (Data Book v2.1)
7	Board Insertion ENUM# Status Indicator	0	1

3. M Mode TEA# Functional Description for PCI 9054 Revision AC

The functionality of TEA# has changed, relative to the *PCI 9054 Data Book, Version 2.1*.

PCI 9054 TEA# Assertion

The PCI 9054 will assert the TEA# signal in response to Master Aborts, Target Aborts, and other specified error conditions that may occur during Direct Master Reads or Writes, Configuration Reads or Writes, or DMA accesses.

Depending upon the error/abort condition and when it is detected, TEA# will either be asserted during the currently active local bus transfer or when the Motorola MPC860 returns to attempt a new Direct Master Read/Write, Configuration Read/Write, or DMA transfer, or resumes a Deferred Read.

When it is asserted, TEA# is always a one-clock-pulse-wide signal, synchronous to the rising edge of the clock.

When enabled (INTCSR[0]=1), TEA# will be asserted under the following error/abort conditions:

1. A Master Abort condition occurs (PCISR[13]=1) during a Direct Master Read/Write, Configuration Read/Write, or DMA transfer.

2. A Target Abort is received (PCISR[12]=1) during a Direct Master Read/Write, Configuration Read/Write, or DMA transfer.

3. A transfer is Retried 256 times by the Target (PCISR[12]=1) during a Direct Master Read/Write, Configuration Read/Write, or DMA transfer.

TEA# will be asserted, regardless of the Deferred Read Enable bit (LMISC[4]) setting.

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The PCI 9054 can assert TEA# any time during the transfer, following the clock period during which TS# was asserted, as illustrated in Figure 1.

Figure 1. Normally Terminated Bus Transfer
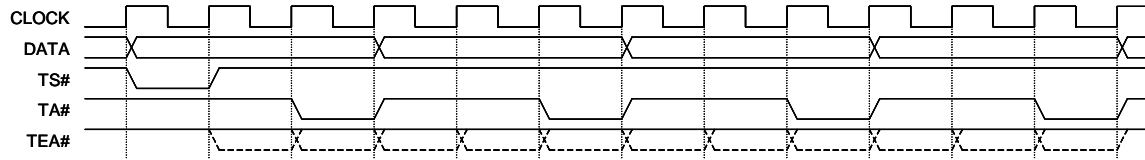
The PCI 9054 can assert TEA# at the same time as TA# to abort the transfer, as illustrated in Figure 2.

Figure 2. Transfer Aborted with TEA# and TA# Assertion
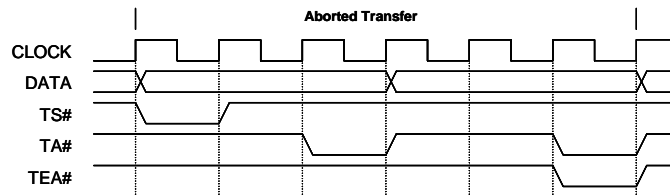
The PCI 9054AC can assert TEA# to abort the transfer before TA# would have been asserted. When this occurs, TA# will not be asserted until a new transfer begins, as illustrated in Figure 3.

Figure 3. Transfer Aborted with TEA# Asserted before TA#

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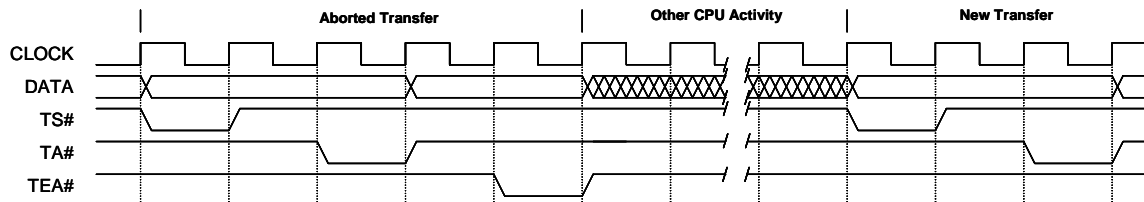
Using LINT# with TEA#

The PCI 9054 will assert the LINT# signal under the following circumstances:

1. Messaging Queue outbound overflow or inbound not empty.

2. DMA Channel 0 or 1 Transfer is done or has reached a terminal count.

3. A Local or PCI Parity error has been detected.

4. A Doorbell, BIST, Mailbox, or Power Management interrupt has been set.

5. A Master Abort (No DEVSEL) was received during a Direct Master Read/Write, Configuration Read/Write, or DMA transfer.

6. A Target Abort was received or 256 Retries was detected during a Direct Master Read/Write, Configuration Read/Write, or DMA transfer.

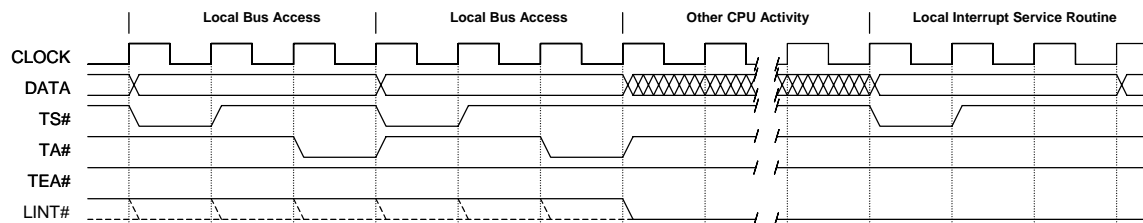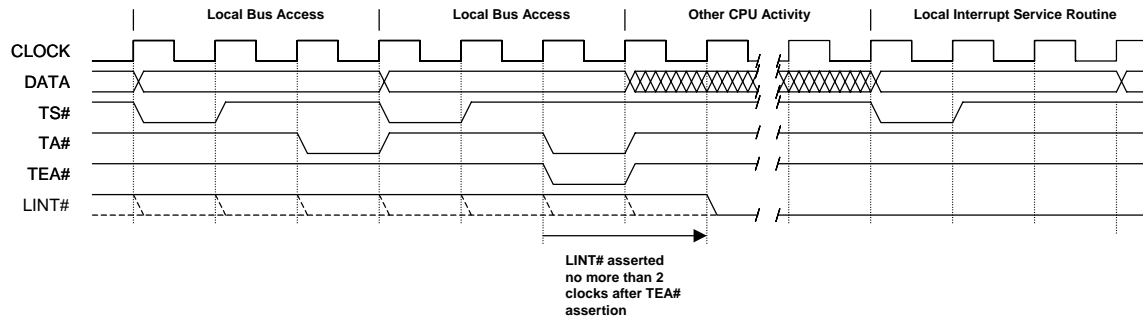Unlike TEA#, LINT# can be asserted at any time, even when the PCI 9054 is not performing a local bus transfer, as illustrated in Figure 4.

Figure 4. LINT# Assertion without TEA#

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If TEA# is asserted during a local bus transfer, LINT# will be asserted within two clock cycles, as illustrated in Figure 5.

Figure 5. LINT# Assertion with TEA#

If the Abort bits PCISR[13:12] that caused LINT# are cleared before a Direct Master Read/Write, Configuration Read/Write, or DMA transfer is attempted, the new transfer will proceed normally (TEA# is not issued).

PCI 9054 Response to a TEA# Assertion – Bus Monitor Timeout

The Motorola MPC860 can (if programmed to do so) assert TEA# as a Master or Slave if its Bus Monitor times out:

1. If TEA# is asserted by the MPC860 while the PCI 9054 is the local bus master, TEA# will pre-empt the TA# input and terminate the current cycle. If the burst is not completed, the PCI 9054 will generate a new TS# and continue. This applies for Direct Slave and DMA transfers.

2. If TEA# is asserted by the MPC860 while the PCI 9054 is the local bus slave, the PCI 9054 ignores TEA#.

If LMISC[5]=1, the PCI 9054 can generate an SERR# on the PCI Bus upon detection of TEA# being asserted, as described on page 11-22 of the *PCI 9054 Data Book, Version 2.1*.

4. Addendum to PCN 2005-4

PCI9054-AC50PI devices will no longer be manufactured in body size 24 x 24 x 2.7 mm (QFP18). These devices are being replaced with body size 24 x 24 x 1.4 mm (QFP21) devices, and will be offered with a new ordering code: PCI9054-AC50VPI.

5. PCI 9054 Lead-Free ROHS-Compliant Version Ordering Information

The PCI 9054 is available in standard leaded packaging and lead-free ROHS packaging. Ordering information is delineated in the following table.

Part Number	Package
PCI 9054-AC50PI	Standard Leaded PQFP Package
PCI 9054-AC50PI F	Lead-Free ROHS PQFP Packaging
PCI 9054-AC50BI	Standard Leaded PBGA Package
PCI 9054-AC50BI F	Lead-Free ROHS PBGA Packaging

6. EOL of PCI9054-AC50VPI and package dimensions of PCI9054-AC50PI F

The PCI9054-AC50VPI has gone into EOL stage with a Last time buy date of 09/15/2006 and a last time ship date of 03/30/2007. However PLX will continue to ship the lead-free version PCI9054-AC50PI F and the package dimensions of this lead-free device are 24 x 24 x 1.4 mm (QFP21).

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