User's Manual

NEC

μPD720101

USB 2.0 Host Controller

[MEMO]

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Main Revisions in this Edition

Page	Description
pp.13, 16	Addition of lead-free products
p. 65	Change of description in **4. 2. 3 Overview of OHCI operational registers**
pp. 129 to 131	Change of **Figure 9-1. USB Downstream Port Connection** to **Figure 9-4. External Serial ROM Connection**

The mark ★ shows major revised points.

PREFACE

Readers   This manual is intended for engineers who need to be familiar with the capability of the μPD720101 in order to develop application systems based on it.

Purpose   The purpose of this manual is to help users understand the hardware capabilities (listed below) of the μPD720101.

Configuration   This manual consists of the following chapters:

- Introduction
- Pin functions
- Information for NAND-tree test mode
- Register information
- OHCI host controller
- EHCI host controller
- Power management
- How to write external serial ROM
- How to connect to external elements
- Product specifications

Guidance   Readers of this manual should already have a general knowledge of electronics, logic circuits, and microcomputers.

Notation   This manual uses the following conventions:

Data bit significance:	High-order bits on the left side; low-order bits on the right side
Active low:	XXXX0 (Pin and signal names are suffixed with 0.)
Note:	Explanation of an indicated part of text
Caution:	Information requiring the user's special attention
Remark:	Supplementary information
Numerical value:	Binary ... xxxx or xxxxb
	Decimal ... xxxx
	Hexadecimal ... xxxxh

Related Document   Use this manual in combination with the following document.
The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- μPD720101 Data Sheet: S16265E

CONTENTS

LIST OF FIGURES

LIST OF TABLES (1/2)

CHAPTER 1 INTRODUCTION

The μPD720101 complies with the Universal Serial Bus Specification Revision 2.0 and Open Host Controller Interface Specification for full-/low-speed signaling and Intel's Enhanced Host Controller Interface Specification for high-speed signaling and works up to 480 Mbps. The μPD720101 is integrated 3 host controller cores with PCI Interface and USB 2.0 transceivers into a single chip.

1.1 Features

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data rate 1.5/12/480 Mbps)
- Compliant with Open Host Controller Interface Specification for USB Rev 1.0a
- Compliant with Enhanced Host Controller Interface Specification for USB Rev 1.0
- PCI multi-function device consists of two OHCI host controller cores for full-/low-speed signaling and one EHCI host controller core for high-speed signaling.
- Root hub with 5 (max.) downstream facing ports which are shared by OHCI and EHCI host controller cores.
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Configurable number of downstream facing ports (2 to 5)
- 32-bit 33 MHz host interface compliant to PCI Specification release 2.2
- Supports PCI Mobile Design Guide Revision 1.1
- Supports PCI-Bus Power Management Interface Specification release 1.1
- PCI bus bus-master access
- System clock is generated by 30 MHz X'tal or 48 MHz clock input.
- Operational registers direct-mapped to PCI memory space
- Legacy support for all downstream facing ports. Legacy support features allow easy migration for motherboard implementation.
- 3.3 V power supply, PCI signal pins have 5 V tolerant circuit.

1.2 Ordering Information

Part Number	Package	Remark
μPD720101GJ-UEN	144-pin plastic LQFP (Fine pitch) (20 × 20)	
★ μPD720101GJ-UEN-A	144-pin plastic LQFP (Fine pitch) (20 × 20)	Lead-free product
μPD720101F1-EA8	144-pin plastic FBGA (12 × 12)	
★ μPD720101F1-EA8-A	144-pin plastic FBGA (12 × 12)	Lead-free product

1.3 Block Diagram

PCI Bus

PME0 INTA0   INTB0   INTC0

PCI Bus Interface

WakeUp_Event   WakeUp_Event   WakeUp_Event

Arbiter

OHCI Host Controller #1 OHCI Host Controller #2 EHCI Host Controller

SMI0

Root Hub

PHY

Port 1 Port 2 Port 3 Port 4 Port 5

USB Bus

Remark INTB0/INTC0 can be shared with INTA0 through BIOS setting. (Planning)

PCI Bus Interface	:	handles 32-bit 33 MHz PCI bus master and target function which comply with PCI specification release 2.2. The number of enabled ports is set by bit in configuration space.
Arbiter	:	arbitrates among two OHCI host controller cores and one EHCI host controller core.
OHCI Host Controller #1	:	handles full- (12 Mbps)/low-speed (1.5 Mbps) signaling at port 1, 3, and 5.
OHCI Host Controller #2	:	handles full- (12 Mbps)/low-speed (1.5 Mbps) signaling at port 2 and 4.
EHCI Host Controller	:	handles high- (480 Mbps) signaling at port 1, 2, 3, 4, and 5.
Root Hub	:	handles USB hub function in host controller and controls connection (routing) between host controller core and port.
PHY	:	consists of high-speed transceiver, full-/low-speed transceiver, serializer, deserializer, etc.
INTA0	:	is the PCI interrupt signal for OHCI Host Controller #1.
INTB0	:	is the PCI interrupt signal for OHCI Host Controller #2.
INTC0	:	is the PCI interrupt signal for EHCI Host Controller.
SMI0	:	is the interrupt signal which is specified by Open Host Controller Interface Specification for USB Rev 1.0a and Enhanced Host Controller Interface Specification Rev 1.0. The SMI signal of each OHCI Host Controller and EHCI Host Controller appears at this signal.
PME0	:	is the interrupt signal which is specified by PCI-Bus Power Management Interface Specification release 1.1. Wakeup signal of each host controller core appears at this signal.

COMPARISON WITH THE μPD720100A

	μPD720100A	μPD720101 (2nd generation)
EHCI revision	0.95	1.0
EHCI	1	1
OHCI	2	2
Legacy support	Parallel IRQ out support	No parallel IRQ support
Clock	48 MHz OSC or 30 MHz OSC/X'tal	48 MHz OSC or 30 MHz X'tal
Package	176-pin BGA (FP) or 160-pin LQFP	144-pin BGA (FP) or 144-pin LQFP

1.4 Pin Configuration

- **144-pin plastic LQFP (Fine pitch) (20 × 20)**

  μPD720101GJ-UEN

★ μPD720101GJ-UEN-A

Top View

Top pins (144 → 109): Vss, Vss, RSDP5, DP5, Vdd, DM5, RSDM5, Vss, RSDP4, DP4, Vdd, DM4, RSDM4, Vss, RSDP3, DP3, Vdd, DM3, RSDM3, Vss, Vdd, Vss, Vss, RSDP2, DP2, Vdd, DM2, RSDM2, RSDP1, DP1, Vdd, DM1, RSDM1, Vss, Vss

Left pins (1 → 36): VDD (1), VDD, OCI1, PPON1, OCI2 (5), PPON2, OCI3, PPON3, OCI4, PPON4 (10), OCI5, PPON5, VCCRST0, PME0, PCLK (15), VBBRST0, VDD_PCI, Vss, VDD, INTA0 (20), INTB0, INTC0, GNT0, REQ0, AD31 (25), AD30, AD29, AD28, AD27, AD26 (30), AD25, AD24, CBE30, IDSEL, Vss (35), VDD

Right pins (109 → 72): VDD, AVss, AVDD, AVss (105), AVss(R), RREF, AVDD, Vss, Vss (100), NANDTEST, SRDTA, SRMOD, SRCLK, XT1/SCLK (95), XT2, VDD, NTEST1, TEST, LEGC (90), SMC, TEB, AMC, SMI0, N.C. (85), N.C., CRUN0, AD0, AD1, VDD_PCI (80), AD2, AD3, AD4, AD5, AD6 (75), VDD, VDD

Bottom pins (37 → 71): Vss, Vss, AD23, AD22 (40), AD21, AD20, VDD, AD19, AD18 (45), AD17, AD16, CBE20, FRAME0, IRDY0 (50), TRDY0, DEVSEL0, STOP0, Vss, VDD (55), VDD_PCI, PERR0, SERR0, PAR, CBE10 (60), AD15, AD14, AD13, AD12, AD11 (65), AD10, AD9, AD8, CBE00, AD7 (70), Vss, Vss

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD}	37	V_{SS}	73	V_{DD}	109	V_{SS}
2	V_{DD}	38	V_{SS}	74	V_{DD}	110	V_{SS}
3	OCI1	39	AD23	75	AD6	111	RSDM1
4	PPON1	40	AD22	76	AD5	112	DM1
5	OCI2	41	AD21	77	AD4	113	V_{DD}
6	PPON2	42	AD20	78	AD3	114	DP1
7	OCI3	43	V_{DD}	79	AD2	115	RSDP1
8	PPON3	44	AD19	80	V_{DD_PCI}	116	V_{SS}
9	OCI4	45	AD18	81	AD1	117	RSDM2
10	PPON4	46	AD17	82	AD0	118	DM2
11	OCI5	47	AD16	83	CRUN0	119	V_{DD}
12	PPON5	48	CBE20	84	N.C.	120	DP2
13	VCCRST0	49	FRAME0	85	N.C.	121	RSDP2
14	PME0	50	IRDY0	86	SMI0	122	V_{SS}
15	PCLK	51	TRDY0	87	AMC	123	V_{SS}
16	VBBRST0	52	DEVSEL0	88	TEB	124	V_{DD}
17	V_{DD_PCI}	53	STOP0	89	SMC	125	V_{SS}
18	V_{SS}	54	V_{SS}	90	LEGC	126	RSDM3
19	V_{DD}	55	V_{DD}	91	TEST	127	DM3
20	INTA0	56	V_{DD_PCI}	92	NTEST1	128	V_{DD}
21	INTB0	57	PERR0	93	V_{DD}	129	DP3
22	INTC0	58	SERR0	94	XT2	130	RSDP3
23	GNT0	59	PAR	95	XT1/SCLK	131	V_{SS}
24	REQ0	60	CBE10	96	SRCLK	132	RSDM4
25	AD31	61	AD15	97	SRMOD	133	DM4
26	AD30	62	AD14	98	SRDTA	134	V_{DD}
27	AD29	63	AD13	99	NANDTEST	135	DP4
28	AD28	64	AD12	100	V_{SS}	136	RSDP4
29	AD27	65	AD11	101	V_{SS}	137	V_{SS}
30	AD26	66	AD10	102	AV_{DD}	138	RSDM5
31	AD25	67	AD9	103	RREF	139	DM5
32	AD24	68	AD8	104	$AV_{SS}(R)$	140	V_{DD}
33	CBE30	69	CBE00	105	AV_{SS}	141	DP5
34	IDSEL	70	AD7	106	AV_{DD}	142	RSDP5
35	V_{SS}	71	V_{SS}	107	AV_{SS}	143	V_{SS}
36	V_{DD}	72	V_{SS}	108	V_{DD}	144	V_{SS}

Remark $AV_{SS}(R)$ should be used to connect RREF through 1 % precision reference resistor of 9.1 kΩ.
Pins 84 and 85 must be clamped high on the board.

- **144-pin plastic FBGA (12 × 12)**

    μPD720101F1-EA8

★ μPD720101F1-EA8-A

Bottom View

	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
14		25	26	27	28	29	30	31	32	33	34	35	36		14
13	24	71	72	73	74	75	76	77	78	79	80	81	82	37	13
12	23	70	111	112	113	114	115	116	117	118	119	120	83	38	12
11	22	69	110			137	138	139	140			121	84	39	11
10	21	68	109									122	85	40	10
9	20	67	108	136							141	123	86	41	9
8	19	66	107	135							142	124	87	42	8
7	18	65	106	134							143	125	88	43	7
6	17	64	105	133							144	126	89	44	6
5	16	63	104									127	90	45	5
4	15	62	103		132	131	130	129				128	91	46	4
3	14	61	102	101	100	99	98	97	96	95	94	93	92	47	3
2	13	60	59	58	57	56	55	54	53	52	51	50	49	48	2
1		12	11	10	9	8	7	6	5	4	3	2	1		1
	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	37	V_{DD}	73	V_{DD}	109	NANDTEST
2	AD23	38	V_{DD}	74	RSDP1	110	V_{SS}
3	AD20	39	PPON2	75	V_{DD}	111	AV_{SS}
4	AD18	40	OCI4	76	V_{DD}	112	V_{SS}
5	CBE20	41	PPON5	77	DP3	113	DM2
6	TRDY0	42	PCLK	78	V_{DD}	114	RSDP2
7	SERR0	43	INTC0	79	RSDM5	115	V_{SS}
8	AD15	44	AD31	80	V_{DD}	116	V_{DD}
9	AD12	45	AD28	81	DP5	117	RSDM4
10	AD9	46	AD25	82	V_{SS}	118	DP4
11	AD7	47	V_{DD}	83	OCI1	119	V_{SS}
12	V_{SS}	48	V_{SS}	84	OCI2	120	PPON1
13	V_{DD}	49	V_{SS}	85	OCI3	121	PPON3
14	V_{DD}	50	AD22	86	OCI5	122	PPON4
15	AD3	51	AD21	87	VBBRST0	123	VCCRST0
16	AD1	52	V_{DD}	88	INTB0	124	V_{DD_PCI}
17	N.C.	53	AD16	89	AD30	125	INTA0
18	AMC	54	DEVSEL0	90	AD26	126	REQ0
19	XT2	55	PERR0	91	AD24	127	AD29
20	SRMOD	56	AD14	92	IDSEL	128	AD27
21	V_{SS}	57	AD10	93	CBE30	129	IRDY0
22	RREF	58	AD8	94	AD19	130	V_{SS}
23	V_{DD}	59	CBE00	95	AD17	131	V_{DD}
24	AV_{SS}	60	V_{SS}	96	FRAME0	132	PAR
25	V_{SS}	61	AD6	97	STOP0	133	SMI0
26	RSDM1	62	AD4	98	V_{DD_PCI}	134	LEGC
27	DP1	63	AD2	99	CBE10	135	TEST
28	RSDM2	64	CRUN0	100	AD13	136	XT1/SCLK
29	DP2	65	TEB	101	AD11	137	V_{SS}
30	V_{SS}	66	V_{DD}	102	AD5	138	RSDM3
31	RSDP3	67	SRDTA	103	V_{DD_PCI}	139	DM3
32	DM4	68	AV_{DD}	104	AD0	140	V_{SS}
33	RSDP4	69	$AV_{SS}(R)$	105	N.C.	141	PME0
34	DM5	70	AV_{DD}	106	SMC	142	V_{SS}
35	RSDP5	71	V_{SS}	107	NTEST1	143	V_{DD}
36	V_{SS}	72	DM1	108	SRCLK	144	GNT0

Remark $AV_{SS}(R)$ should be used to connect RREF through 1 % precision reference resistor of 9.1 kΩ.
Pins 17 and 105 must be clamped high on the board.

PIN INFORMATION

(1/2)

Pin Name	I/O	Buffer Type	Active Level	Function
AD (31 : 0)	I/O	5 V PCI I/O		PCI "AD [31 : 0]" signal
CBE (3 : 0)0	I/O	5 V PCI I/O		PCI "C/BE [3 : 0]" signal
PAR	I/O	5 V PCI I/O		PCI "PAR" signal
FRAME0	I/O	5 V PCI I/O		PCI "FRAME#" signal
IRDY0	I/O	5 V PCI I/O		PCI "IRDY#" signal
TRDY0	I/O	5 V PCI I/O		PCI "TRDY#" signal
STOP0	I/O	5 V PCI I/O		PCI "STOP#" signal
IDSEL	I	5 V PCI input		PCI "IDSEL" signal
DEVSEL0	I/O	5 V PCI I/O		PCI "DEVSEL#" signal
REQ0	O	5 V PCI output		PCI "REQ#" signal
GNT0	I	5 V PCI input		PCI "GNT#" signal
PERR0	I/O	5 V PCI I/O		PCI "PERR#" signal
SERR0	O	5 V PCI N-ch open drain		PCI "SERR#" signal
INTA0	O	5 V PCI N-ch open drain	Low	PCI "INTA#" signal
INTB0	O	5 V PCI N-ch open drain	Low	PCI "INTB#" signal
INTC0	O	5 V PCI N-ch open drain	Low	PCI "INTC#" signal
PCLK	I	5 V PCI input		PCI "CLK" signal
VBBRST0	I	5 V tolerant input	Low	Hardware reset for chip
CRUN0	I/O	5 V PCI I/O		PCI "CLKRUN#" signal
PME0	O	5 V PCI N-ch open drain	Low	PCI "PME#" signal
VCCRST0	I	5 V tolerant input	Low	Reset for power management
SMI0	O	5 V tolerant N-ch open drain	Low	System management interrupt output
XT1/SCLK	I	Input		System clock input or oscillator in
XT2	O	Output		oscillator out
DP (5 : 1)	I/O	USB high speed D+ I/O		USB high speed D+ signal
DM (5 : 1)	I/O	USB high speed D− I/O		USB high speed D− signal
RSDP (5 : 1)	O	USB full speed D+ Output		USB full speed D+ signal
RSDM (5 : 1)	O	USB full speed D− Output		USB full speed D− signal
OCI (5 : 1)	I (I/O)	Input	Low	USB root hub port's overcurrent status input
PPON (5 : 1)	O (I/O)	Output	High	USB root hub port's power supply control output
LEGC	I (I/O)	Input	High	Legacy support switch
SRCLK	O	Output		Serial ROM clock out
SRDTA	I/O	I/O		Serial ROM data
SRMOD	I	Input with 50 kΩ pull down R	High	Serial ROM input enable
RREF	A	Analog		Reference resistor
NTEST1	I	Input with 12 kΩ pull down R	High	Test pin

(2/2)

Pin Name	I/O	Buffer Type	Active Level	Function
SMC	I	Input with 50 kΩ pull down R	High	Scan mode control
TEB	I	Input with 50 kΩ pull down R	High	BIST enable
AMC	I	Input with 50 kΩ pull down R	High	ATG mode control
TEST	I	Input with 50 kΩ pull down R	High	Test control
NANDTEST	I	Input with 50 kΩ pull down R	High	NAND tree test enable
AV_{DD}				V_{DD} for analog circuit
V_{DD}				V_{DD}
V_{DD_PCI}				5 V (5 V PCI) or 3.3 V (3.3 V PCI)
AV_{SS}				V_{SS} for analog circuit
V_{SS}				V_{SS}
N.C.				No connection

Remarks 1. "5 V tolerant" means that the buffer is 3 V buffer with 5 V tolerant circuit.

2. "5 V PCI" indicates a PCI buffer, which complies with the 3 V PCI standard, has a 5 V tolerant circuit. It does not indicate that this buffer fully complies with 5 V PCI standard. However, this function can be used for evaluating the operation of a device on a 5 V add-in card.

3. The signal marked as "(I/O)" in the above table operates as I/O signals during testing. However, they do not need to be considered in normal use.

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Functions for 144-pin LQFP

The pin type describes a signal either as analog, power, input, or I/O (bi-directional).

2.1.1 Power supply

Pin	Pin No.	Direction	Function
V_{DD}	1, 2, 19, 36, 43, 55, 73, 74, 93, 108, 113, 119, 124, 128, 134, 140	Power	+3.3 V power supply
V_{DD_PCI}	17, 56, 80	Power	+5 V for 5 V PCI or +3.3 V for 3.3 V PCI
AV_{DD}	102, 106	Power	+3.3 V power supply for analog circuit
V_{SS}	18, 35, 37, 38, 54, 71, 72, 100, 101, 109, 110, 116, 122, 123, 125, 131, 137, 143, 144	Power	Ground
AV_{SS}	104, 105, 107	Power	Ground for analog circuit
N.C.	84, 85	-	These N.C. pins must be pulled high on the board.

2.1.2 Analog signaling

Pin	Pin No.	Direction	Function
RREF	103	Analog	RREF must be connected a 1% precision reference resistor of 9.1 kΩ. The other side of resistor must be connected to local ground.

2.1.3 PCI interface

Pin	Pin No.	Direction	Function
AD (31 : 0)	25, 26, 27, 28, 29, 30, 31, 32, 39, 40, 41, 42, 44, 45, 46, 47, 61, 62, 63, 64, 65, 66, 67, 68, 70, 75, 76, 77, 78, 79, 81, 82	I/O	PCI "AD [31 : 0]" signal
CBE (3 : 0)0	33, 48, 60, 69	I/O	PCI "C/BE [3 : 0]" signal
PAR	59	I/O	PCI "PAR" signal
FRAME0	49	I/O	PCI "FRAME#" signal
IRDY0	50	I/O	PCI "IRDY#" signal
TRDY0	51	I/O	PCI "TRDY#" signal
STOP0	53	I/O	PCI "STOP#" signal
IDSEL	34	I	PCI "IDSEL" signal
DEVSEL0	52	I/O	PCI "DEVSEL#" signal
REQ0	24	O	PCI "REQ#" signal
GNT0	23	I	PCI "GNT#" signal
PERR0	57	I/O	PCI "PERR#" signal
SERR0	58	O	PCI "SERR#" signal
INTA0	20	O	PCI "INTA#" signal
INTB0	21	O	PCI "INTB#" signal
INTC0	22	O	PCI "INTC#" signal
PCLK	15	I	PCI "CLK" signal
VBBRST0	16	I	Hardware reset for Chip
CRUN0	83	I/O	PCI "CLKRUN#" signal
PME0	14	O	PCI "PME#" signal

Remarks 1. For details of PCI operations, see the **PCI Local Bus Specification Revision 2.2**.

2. See **CHAPTER 7 POWER MANAGEMENT** to decide the setting of VBBRST0. The setting of this signal is decided by power management support level.

2.1.4 System clock & reset for power management

Pin	Pin No.	Direction	Caution
XT1/SCLK	95	I	System clock input or Oscillator input Apply 48-MHz clock input or connect to 30-MHz X'tal. Clock frequency is selected by "Clock_sel reg." in EXT2.
XT2	94	O	If 48-MHz clock input is applied to SCLK, this signal must be opened. Otherwise, connect to 30-MHz X'tal. Clock frequency is selected by "Clock_sel reg." in EXT2.
VCCRST0	13	I	Reset for power management.

Remark See **CHAPTER 7 POWER MANAGEMENT** to decide the setting of VCCRST0. The setting of this signal is decided by power management support level.

2.1.5 USB interface

Pin	Pin No.	Direction	Function
DP (5 : 1)	141, 135, 129, 120, 114	I/O	USB D+ high-speed signal Shared with DMx pins having the same numbers.
RSDP (5 : 1)	142, 136, 130, 121, 115	O	USB D+ full-speed signal Connected to DPx through 36 Ω 1% precision Rs resistor.
DM (5 : 1)	139, 133, 127, 118, 112	I/O	USB D− high-speed signal Shared with DPx pins having the same numbers.
RSDM (5 : 1)	138, 132, 126, 117, 111	O	USB D− full-speed signal Connected to DMx through 36 Ω 1% precision Rs resistor.
OCI (5 : 1)	11, 9, 7, 5, 3	I	Pin for inputting the overcurrent status of the USB Root Hub Port 1: No power supply problem 0: Overcurrent has occurred
PPON (5 : 1)	12, 10, 8, 6, 4	O	Power supply control output for USB Root Hub Port 0: Power supply OFF 1: Power supply ON

2.1.6 Legacy support interface

Pin	Pin No.	Direction	Function
LEGC	90	I	Legacy support switch 0: Legacy OFF 1: Legacy ON
aDDITIOSMI0	86	O	System management interrupt output 0: Interrupt occurs 1: Interrupt does not occur

2.1.7 Serial ROM interface

Pin	Pin No.	Direction	Caution
SRCLK	96	O	Serial ROM Clock Out
SRDTA	98	I/O	Serial ROM Data
SRMOD	97	I	Serial ROM Input Enable 0 (default): Serial ROM Inactive 1: Serial ROM Active

2.1.8 Test signals

Pin	Pin No.	Direction	Caution
SMC	89	I	Should be left open on circuit board.
AMC	87	I	Should be left open on circuit board.
NANDTEST	99	I	NAND-Tree test enable. 0 (default): NAND-Tree test disable 1: NAND-Tree test enable This can be left open on circuit board.
TEB	88	I	Should be left open on circuit board.
TEST	91	I	Should be left open on circuit board.
NTEST1	92	I	Should be left open on circuit board.

2.2 Pin Functions for 144-pin FBGA

The pin type describes a signal either as analog, power, input, or I/O (bi-directional).

2.2.1 Power supply

Pin	Pin No.	Direction	Function
V_{DD}	13, 14, 23, 37, 38, 47, 52, 66, 73, 75, 76, 78, 80, 116, 131, 143	Power	+3.3 V power supply
V_{DD_PCI}	98, 103, 124	Power	+5 V for 5 V PCI or +3.3 V for 3.3 V PCI
AV_{DD}	68, 70	Power	+3.3 V power supply for analog circuit
V_{SS}	1, 12, 21, 25, 30, 36, 48, 49, 60, 71, 82, 110, 112, 115, 119, 130, 137, 140, 142	Power	Ground
AV_{SS}	24, 69, 111	Power	Ground for analog circuit
N.C.	17, 105	-	These N.C. pins must be pulled high on the board.

2.2.2 Analog signaling

Pin	Pin No.	Direction	Function
RREF	22	Analog	RREF must be connected a 1% precision reference resistor of 9.1 kΩ. The other side of resistor must be connected to local ground.

2.2.3 PCI interface

Pin	Pin No.	Direction	Function
AD (31 : 0)	44, 89, 127, 45, 128, 90, 46, 91, 2, 50, 51, 3, 94, 4, 95, 53, 8, 56, 100, 9, 101, 57, 10, 58, 11, 61, 102, 62, 15, 63, 16, 104	I/O	PCI "AD [31 : 0]" signal
CBE (3 : 0)0	93, 5, 99, 59	I/O	PCI "C/BE [3 : 0]" signal
PAR	132	I/O	PCI "PAR" signal
FRAME0	96	I/O	PCI "FRAME#" signal
IRDY0	129	I/O	PCI "IRDY#" signal
TRDY0	6	I/O	PCI "TRDY#" signal
STOP0	97	I/O	PCI "STOP#" signal
IDSEL	92	I	PCI "IDSEL" signal
DEVSEL0	54	I/O	PCI "DEVSEL#" signal
REQ0	126	O	PCI "REQ#" signal
GNT0	144	I	PCI "GNT#" signal
PERR0	55	I/O	PCI "PERR#" signal
SERR0	7	O	PCI "SERR#" signal
INTA0	125	O	PCI "INTA#" signal
INTB0	88	O	PCI "INTB#" signal
INTC0	43	O	PCI "INTC#" signal
PCLK	42	I	PCI "CLK" signal
VBBRST0	87	I	Hardware reset for Chip
CRUN0	64	I/O	PCI "CLKRUN#" signal
PME0	141	O	PCI "PME#" signal

Remarks 1. For details of PCI operations, see the **PCI Local Bus Specification Revision 2.2**.

2. See **CHAPTER 7 POWER MANAGEMENT** to decide the setting of VBBRST0. The setting of this signal is decided by power management support level.

2.2.4 System clock & reset for power management

Pin	Pin No.	Direction	Caution
XT1/SCLK	136	I	System clock input or Oscillator input Apply 48-MHz clock input or connect to 30-MHz X'tal. Clock frequency is selected by "Clock_sel reg." in EXT2.
XT2	19	O	If 48-MHz clock input is applied to SCLK, this signal must be opened. Otherwise, connect to 30-MHz X'tal. Clock frequency is selected by "Clock_sel reg." in EXT2.
VCCRST0	123	I	Reset for power management.

Remark See **CHAPTER 7 POWER MANAGEMENT** to decide the setting of VCCRST0. The setting of this signal is decided by power management support level.

2.2.5 USB interface

Pin	Pin No.	Direction	Function
DP (5 : 1)	81, 118, 77, 29, 27	I/O	USB D+ high-speed signal Shared with DMx pins having the same numbers.
RSDP (5 : 1)	35, 33, 31, 114, 74	O	USB D+ full-speed signal Connected to DPx through 36 Ω 1% precision Rs resistor.
DM (5 : 1)	34, 32, 139, 113, 72	I/O	USB D− high-speed signal Shared with DPx pins having the same numbers.
RSDM (5 : 1)	79, 117, 138, 28, 26	O	USB D− full-speed signal Connected to DMx through 36 Ω 1% precision Rs resistor.
OCI (5 : 1)	86, 40, 85, 84, 83	I	Pin for inputting the overcurrent status of the USB Root Hub Port 1: No power supply problem 0: Overcurrent has occurred
PPON (5 : 1)	41, 122, 121, 39, 120	O	Power supply control output for USB Root Hub Port 0: Power supply OFF 1: Power supply ON

2.2.6 Legacy support interface

Pin	Pin No.	Direction	Function
LEGC	134	I	Legacy support switch 0: Legacy OFF 1: Legacy ON
SMI0	133	O	System management interrupt output 0: Interrupt occurs 1: Interrupt does not occur

2.2.7 Serial ROM interface

Pin	Pin No.	Direction	Caution
SRCLK	108	O	Serial ROM Clock Out
SRDTA	67	I/O	Serial ROM Data
SRMOD	20	I	Serial ROM Input Enable 0 (default): Serial ROM Inactive 1: Serial ROM Active

2.2.8 Test signals

Pin	Pin No.	Direction	Caution
SMC	106	I	Should be left open on circuit board.
AMC	18	I	Should be left open on circuit board.
NANDTEST	109	I	NAND-Tree test enable. 0 (default): NAND-Tree test disable 1: NAND-Tree test enable This can be left open on circuit board.
TEB	65	I	Should be left open on circuit board.
TEST	135	I	Should be left open on circuit board.
NTEST1	107	I	Should be left open on circuit board.

CHAPTER 3 INFORMATION FOR NAND-TREE TEST MODE

The μPD720101 supports NAND-Tree test mode. NAND-Tree test mode is for testing connection on board. When NANDTEST is set to "high", NAND-Tree test mode is enabled and all of listed bi-directional signals are configured as input mode. And all of listed output signals except for NAND-Tree's output buffer are configured as high-impedance state. The following table lists each NAND-Tree pin ordering, with the first value being the first input and the last value being the NAND-Tree output.

There are two methods for performing NAND-Tree test.
- At first, all NAND-Tree input pins should be set to "low". At that time, the output of the NAND-Tree will be "high". Starting at the last signal on the NAND-Tree (signal at bottom of list next to output), set to "1" onto each signal, one at a time. The NAND-Tree output will be toggled when each input signal transitions from "low" to "high". The maximum propagation delay from input signals to NAND-Tree output is 25 ns.

- The second method works in reverse. Set all NAND-Tree input pins "high". Then starting at the first signal on the NAND-Tree (signal at top of list), set to "0" onto each signal, one at a time. The NAND-Tree output will toggled on each input signal transitions from "high" to "low". The propagation delay from input signals to NAND-Tree output is 25 ns.

Figure 3-1. NAND-Tree Circuitry

Table 3-1. NAND Tree Pin List

Pin No.	Pin Name	I/O	QFP Pin	BGA Ball	Note	Pin No.	Pin Name	I/O	QFP Pin	BGA Ball	Note
1	LEGC	I/O	90	L7		31	STOP0	I/O	53	G3	
2	VCCRST0	I	13	C9		32	PERR0	I/O	57	H2	
3	N.C.	I/O	84	P6		33	PAR	I/O	59	J4	
4	N.C.	I/O	85	M6		34	CBE10	I/O	60	J3	
5	PCLK	I	15	A8		35	AD15	I/O	61	J1	
6	VBBRST0	I	16	B8		36	AD14	I/O	62	J2	
7	GNT0	I	23	D6		37	AD13	I/O	63	K3	
8	AD31	I/O	25	A6		38	AD12	I/O	64	K1	
9	AD30	I/O	26	B6		39	AD11	I/O	65	L3	
10	AD29	I/O	27	C5		40	AD10	I/O	66	K2	
11	AD28	I/O	28	A5		41	AD9	I/O	67	L1	
12	AD27	I/O	29	C4		42	AD8	I/O	68	L2	
13	AD26	I/O	30	B5		43	CBE00	I/O	69	M2	
14	AD25	I/O	31	A4		44	AD7	I/O	70	M1	
15	AD24	I/O	32	B4		45	AD6	I/O	75	N3	
16	CBE30	I/O	33	C3		46	AD5	I/O	76	M3	
17	IDSEL	I	34	B3		47	AD4	I/O	77	N4	
18	AD23	I/O	39	C1		48	AD3	I/O	78	P4	
19	AD22	I/O	40	C2		49	AD2	I/O	79	N5	
20	AD21	I/O	41	D2		50	AD1	I/O	81	P5	
21	AD20	I/O	42	D1		51	AD0	IO	82	M5	
22	AD19	I/O	44	D3		52	CRUN0	IO	83	N6	
23	AD18	I/O	45	E1		53	OCI1	I/O	3	B12	
24	AD17	I/O	46	E3		54	OCI5	I/O	11	B9	
25	AD16	I/O	47	F2		55	OCI2	I/O	5	B11	
26	CBE20	I/O	48	F1		56	OCI4	I/O	9	A10	
27	FRAME0	I/O	49	F3		57	AMC	I	87	P7	
28	IRDY0	I/O	50	F4		58	OCI3	I/O	7	B10	
29	TRDY0	I/O	51	G1		59	SRDTA	I/O	98	N9	NAND-Tree out
30	DEVSEL0	I/O	52	G2							

CHAPTER 4 REGISTER INFORMATION

The μPD720101 consists of two Open HCI (OHCI) Host Controller cores and one Enhanced HCI (EHCI) Host Controller core. OHCI Host Controllers handle full-speed and low-speed device (USB1.x compliant device), which is connected to root hub port on μPD720101. On the other hand, EHCI host controller handles high-speed device (USB2.0 compliant device), which is connected to root hub port on μPD720101. The following sections show PCI configuration space and register information for each host controller. The number of valid ports is controlled by "EXT1" register in EHCI's (OHCI #1's) configuration space.

4.1 PCI Configuration Space

The configuration registers are accessed in order to set up hardware resources, device characteristics or operations, etc. in PCI Local Bus. The following sections describe the PCI Configuration Space, which is the address space for the configuration register. For a more detailed description, see the **PCI Local Bus Specification Revision 2.2.** The settings in PCI configuration space of one Host Controller core are independent of the setting in PCI configuration space of the others without "EXT" register respectively. For example, if "Bus Master" bit in command register of OHCI Host Controller #1 is set to "0", the bus master function of the OHCI Host Controller #1 will be disabled. At that time, if "Bus Master" bit in command register of OHCI Host Controller #2 is set to "1", the bus master function of OHCI Host Controller #2 will be enabled. This functionality in ECHI is the same as in OHCI Host Controller #1 and #2. All corresponding bits shall be set accordingly for enabling/disabling individual host controller.

Table 4-1. Function No. List

Function	Function number	Supported port
OHCI Host Controller #1	0	Port 1, 3, and 5
OHCI Host Controller #2	1	Port 2 and 4
EHCI Host Controller	2	Port 1, 2, 3, 4, and 5

4.1.1 PCI configuration space for OHCI host controller #1

Table 4-2. Configuration Space for OHCI Host Controller #1

31 24	23 16	15 8	7 0	Offset
Device ID		Vender ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
BAR_OHCI Register				10h
I/O Address Register				14h
Reserved				18h
				1Ch
				20h
				24h
Reserved				28h
Subsystem ID		Subsystem Vender ID		2Ch
Expansion ROM Base Address				30h
Reserved			Cap_ptr	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
PMC		Next_Item_Ptr	Cap_ID	40h
Data	PMCSR_BSE	PMCSR		44h
Reserved				46h
				….
				DCh
EXT1				E0h
EXT2				E4h

Table 4-3. Register Information

Register	Address	bits	Read/Write	Value (Default)	Comment
Vender ID	00h	15 : 0	R	1033h	NEC's vendor ID
Device ID	02h	15 : 0	R	0035h	NEC OHCI's device ID
Command	04h	15 : 0			See **Table 4-4.**
Status	06h	15 : 0			See **Table 4-5.**
Revision ID	08h	7 : 0	R	43h	Revision ID
Class Code -Base Class	09h	23 : 16	R	0Ch	Serial Bus Controller Device
-Sub_Class		15 : 8	R	03h	USB Device
-Programming Interface		7 : 0	R	10h	Open HCI Host Controller
Cache Line Size	0Ch	7 : 0	R/W	00h	Cache Line Size
Latency Timer	0Dh	7 : 2	R/W	000010b	Latency Timer for this PCI bus master [Note]
		1 : 0	R	00b	
Header Type	0Eh	7 : 0	R	80h	This is PCI Multi-function.
BIST	0Fh	7 : 0	R	00h	BIST is not supported.
Base Address Register	10h	31 : 0			See **Table 4-6.**
I/O Address Register	14h	31 : 0			See **Table 4-7.**
Subsystem Vender ID	2Ch	15 : 0	R (/W)	1033h	Indicates Subsystem Vender ID
Subsystem ID	2Eh	15 : 0	R (/W)	0035h	Indicates Subsystem ID
Expansion ROM Base Address	30h	31 : 0	R	0000h	Expansion ROM address
Cap_ptr	34h	7 : 0	R	40h	Indicates Capability List header
Interrupt Line	3Ch	7 : 0	R/W	00h	Indicates interrupt line's route
Interrupt Pin	3Dh	7 : 0	R	01h	Routing to INTA0
Min_Gnt	3Eh	7 : 0	R (/W)	01h	Minimum request for burst period.
Max_Lat	3Fh	7 : 0	R (/W)	2Ah	Frequency request of PCI access
Cap_ID	40h	7 : 0	R	01h	ID for PCI Power Management reg.
Next_Item_Ptr	41h	7 : 0	R	00h	There is no next item in the list.
PMC	42h	15 : 0			See **Table 4-8.**
PMCSR	44h	15 : 0			See **Table 4-9.**
PMCSR_BSE	46h	7 : 0	R	00h	Not PCI-to-PCI bridge device
Data	47h	7 : 0	R	00h	No support
EXT1	E0h	32 : 0			See **Table 4-10.**
EXT2	E4h	32 : 0			See **Table 4-11.**

Note This register should be set by system (OS). However, some system may not set this register. So, default value of this register is 08h.

Remark The register marked as "(/W)" in the above table can be written by BIOS when ID_Write_Enable in EHCI's (OHCI #1's) configuration space is set to "1". On the other, the value of these registers can be loaded from external serial ROM with I²C I/F before starting PCI configuration registers access if serial ROM is available.

Table 4-4. Command Register

Field	bit	Read/ Write	Value (Default)	Comment
I/O space	0	R/W	0b	Controls response to I/O access 0: I/O access disable 1: I/O access enable After reset, this bit is set to "0". When "LEGC" pin is "low" or Legc_mode bit in EXT1 Reg. is set to "0", this bit can not be set to "1".
Memory space	1	R/W	0b	Controls response to memory access 0: Memory access disable 1: Memory access enable After reset, this bit is set to "0".
Bus Master	2	R/W	0b	Controls bus master operation 0: Bus master functionality disable 1: Bus master functionality enable After reset, this bit is set to "0".
Special Cycles	3	R	0b	Ignores special cycles
Memory write and invalidate enable	4	R/W	0b	Enables memory write and invalidate command. 0: Memory write and invalidate command disable 1: Memory write and invalidate command enable After reset, this bit is set to "0".
VGA palette snoop	5	R	0b	Sets VGA palette snoop as invalid
Parity Error response	6	R/W	0b	Controls response to parity error. 0: PERR0 can not assert. 1: PERR0 can assert. Even this bit is set to "0", when parity error is detected, Detected parity error bit in Status Reg. is set to "1". After reset, this bit is set to "0".
Wait cycle control	7	R	0b	Address/data stepping is not supported.
SERR# enable	8	R/W	0b	Controls response to system errors. 0: SERR0 can not assert. 1: SERR0 can assert. After reset, this bit is set to "0".
Fast back-to-back enable	9	R	0b	Fast back-to-back access is not supported.
Reserved	15 : 10	R	000000b	Reserved

Table 4-5. Status Register

Field	bit	Read/ Write	Value	Comment
Reserved	3 : 0	R	0000b	Reserved
Capabilities List	4	R	1b	Supports Power Management
66 MHz capable	5	R	0b	33-MHz operation
Reserved	6	R	0b	Reserved
Fast back-to-back capable	7	R	0b	Fast back-to-back access is not supported.
Data Parity Error detected	8	R/W		"High" is set to this bit when the following three conditions are met. (1) PERR0 is asserted by the parity error or assertion of PERR0 was detected. (2) The parity error source was the bus master during the bus cycle in which the parity error occurred. (3) "High" has been set to the command register's Parity Error response bit. This bit can be cleared by set to "1" from PCI.
DEVSEL timing	10 : 9	R	01b	DEVSEL0 assert timing: Medium speed
Signaled target abort	11	R/W		The target sets to "1" whenever it terminates a transaction with Target-abort. This bit can be cleared by set to "1" from PCI.
Received target abort	12	R/W		The master sets to "1" whenever its transaction is terminated with Target-abort. This bit can be cleared by set to "1" from PCI.
Received master abort	13	R/W		The master sets to "1" whenever it terminates a transaction with Master-abort. This bit can be cleared by set to "1" from PCI.
Signaled system error	14	R/W		"High" is set to this bit when SERR0 is asserted. This bit can be cleared by set to "1" from PCI.
Detected parity error	15	R/W		"High" is set to this bit when Address/Data parity error is detected even Parity Error response bit in Command Reg. is set to "0". This bit can be cleared by set to "1" from PCI.

Table 4-6. Base Address (BAR_OHCI) Register

Field	bit	Read/ Write	Value (Default)	Comment
Memory space indicator	0	R	0b	Operational registers are mapped to main memory space.
Type	2 : 1	R	00b	Operational registers can be allocated in any part of the 4-G main memory space.
Prefetchable	3	R	0b	Prefetch is disabled.
Base address (LSB)	11 : 4	R	00h	Operational registers have a 4-Kbyte address space.
Base address (MSB)	31 : 12	R/W	000h	Indicates the high-order 20 bits of the base address in the Operational registers.

Table 4-7. I/O Address Register

Field	bit	Read/ Write	Value (Default)	Comment
I/O space indicator	0	R	Xb	Legacy register is mapped to the I/O space.
Reserved	1	R	0b	Reserved
Base address (LSB)	2	R	0b	Legacy register has an 8-byte address space.
Base address (MSB)	31 : 3	R/W	000h	When Legc_mode bit is set to "0", this register is set to "000"h. And it can not be written by any value. If Legc_mode bit is set to "1", this register will be writtable. This Indicates the high-order 29 bits of the base address in the Legacy register.

Remarks 1. When Legc_mode bit in EXT1 Reg. is set to "0", I/O space indicator is set to "0". And when Legc_mode bit in EXT1 Reg. is set to "1", I/O space indicator indicates the value of "LEGC" pin. At this time, If "LEGC" pin is "low", I/O space indicator will be "0". And if "LEGC" pin is "high", I/O space indicator will be "1".

2. There are two OHCI Host controller cores and one legacy function controller in this chip. The I/O Address in OHCI Host Controller #1 is for legacy function controller. All downstream facing ports can handle legacy functionality. Note that legacy function controller should be shared by two OHCI Host Controllers.

Table 4-8. Power Management Capabilities (PMC) Register

Field	bit	Read/ Write	Value (Default)	Comment
Version	2 : 0	R	010b	PCI Power Management Interface Specification release 1.1
PME Clock	3	R	0b	PCLK is not required for PME0 assertion.
Reserved	4	R	0b	Reserved
DSI	5	R	0b	Does not required Specific Initialization before the generic class device driver is able to use it.
Aux_Current	8 : 6	R (/W)	000b	Indicates current requirement If PME0 generation from $D3_{cold}$ is not supported by this host controller core, this field must return a value of "000b" when read. If PME0 generation from $D3_{cold}$ is supported by this host controller core, following assignments apply: Bit 3.3Vaux 8 7 6 Max. Current Required 1 1 1 375 mA 1 1 0 320 mA 1 0 1 270 mA 1 0 0 220 mA 0 1 1 160 mA 0 1 0 100 mA 0 0 1 55 mA 0 0 0 0 (self powerd)
D1_support	9	R	1b	Support D1 Power Management State
D2_support	10	R	1b	Support D2 Power Management State
PME_support	15	R (/W)	0b	Indicates whether $D3_{cold}$ is supported or not.
	14 : 11	R	1111b	PME0 can be asserted from D0, D1, D2, $D3_{hot}$.

Remark The register marked as "(/W)" in the above table can be written by BIOS when ID_Write_Enable bit is set to "1". On the other, the value of these registers can be loaded from external serial ROM with I^2C I/F before starting PCI configuration registers access if serial ROM is available.

Table 4-9. Power Management Control/Status (PMCSR) Register

Field	bit	Read/ Write	Value (Default)	Comment
Power State	1 : 0	R/W	00b	Shows power state of a host controller core and sets the host controller core into a new power state. 00b: D0 01b: D1 10b: D2 11b: D3$_{hot}$
Reserved	7 : 2	R	00h	Reserved
PME_En	8	R/W	0b	Enable to assert PME0. 0: PME0 assertion disable 1: PME0 assertion enable This bit default to "0" if the host controller core does not support PME0 generation from D3$_{cold}$. If the host controller core supports PME0 generation from D3$_{cold}$, then this bit is sticky and must be explicitly cleared by the OS each time it is initially loaded.
Data_Select	12 : 9	R	0000b	Data register is not implemented.
Data_Scale	14 : 13	R	00b	Data register is not implemented.
PME_Status	15	R/W	0b	PME_Status is set to "1" when ResumeDetected (RD) bit of HcInterruptStatus Reg. in OHCI is set to "1" even PME_En bit is set to "0". This bit can be cleared by set to "1" from PCI. This bit defaults to "0" if the host controller core does not support PME0 generation from D3$_{cold}$. If the host controller core supports PME0 generation from D3$_{cold}$, then this bit is sticky and must be explicitly cleared by the OS each time it is initially loaded.

Remark When Power State is not "D0", the function assumes that it is in Global Suspend and internal clock is stopped.

Table 4-10. EXT1 Register

Field	bit	Read/Write	Value (Default)	Comment
Port No	2 : 0	R/W	5h	Configures valid port number. Value Active ports 5h Port 1, 2, 3, 4, and 5 4h Port 1, 2, 3, and 4 3h Port 1, 2, and 3 2h Port 1 and 2 Prohibited setting the value except for above mentioned.
Legc_mode	3	R/W	0b	Controls the decoding for I/O access to 60h/64h. 0: The HC intercepts 60h/64h access without PCI I/O address space. 1: The HC intercepts 60h/64h access using PCI I/O address space which is indicated in I/O address register of OHCI #1's configuration space. When "LEGC" pin is "low", the setting of this bit is ignored.
NEC private #1	4	R/W	0b	Prohibited setting to "1".
NEC private #2	5	R/W	0b	Prohibited setting to "1".
NEC private #3	6	R/W	0b	Prohibited setting to "1".
ID_Wirte_Enable	7	R/W	0b	Write protection of Subsystem ID and Subsystem Vendor ID, etc. 0: Write Mask 1: Write Enable
NEC private #4	11 : 8	R/W	3h	Prohibited setting the value except for "3h".
NEC private #5	15 : 12	R/W	3h	Prohibited setting the value except for "3h".
NEC private #6	20 :16	R/W	10h	Prohibited setting the value except for "10h".

PPC_setting	21	R/W	1b	Set PPC bit in HCSPARAMS reg.
				
				0: PPC is set to a zero.
				   HC does not have the port power control switches. And then, port power is always active.
				1: PPC is set to a one.
				   HC has the port power control switches.
				
				If port power is always active, this bit should be set to a zero and NPS bit in OHCI's HcRhDescriptorA reg. should be set to a one.

NEC private #7	22	R/W	0b	Prohibited setting to "1".
NEC private #9	23	R	1b	
NEC private #8	31 : 24	R/W	6Ch	Prohibited setting the value except for "6Ch".

Remarks 1. The value of these registers except for ID_Wirte_Enable bit can be loaded from external serial ROM with I²C I/F before starting PCI configuration registers access if serial ROM is available.

2. This register equals to EXT1 register which is indicated in EHCI configuration space. So, This register can be accessed by offset address E0h of EHCI configuration register.

Table 4-11. EXT2 Register

Field	bit	Read/ Write	Value (Default)	Comment
Ehci_mask	0	R/W	0b	Enables EHCI host controller 0: EHCI host controller is enable. 1: EHCI host controller is disable. All PCI access (configuration and memory) to EHCI related space is ignored and EHCI does not work.
NEC private #10	4:1	R/W	0h	Prohibited setting the value except for "0h".
Clock_sel	5	R/W	0b	0: System clock is 30-MHz X'tal. 1: System clock is 48-MHz Oscillator.
NEC private #11	6	R/W	0b	Prohibited setting to "1".
Reserved	31 : 7	R	000h	Reserved

Remark This register except Ehci_mask bit can be accessed by offset address E4h of EHCI configuration register. NEC strongly recommends to set "1" in Ehci_mask bit, when EHCI function is not used.

4.1.2 PCI configuration space for OHCI host controller #2

Table 4-12. Configuration Space for OHCI Host Controller #2

31 24	23 16	15 8	7 0	Offset
Device ID		Vender ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
BAR_OHCI Register				10h
Reserved				14h
				18h
				1Ch
				20h
				24h
Reserved				28h
Subsystem ID		Subsystem Vender ID		2Ch
Expansion ROM Base Address				30h
Reserved			Cap_ptr	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
PMC		Next_Item_Ptr	Cap_ID	40h
Data	PMCSR_BSE	PMCSR		44h

Table 4-13. Register Information

Register	Address	bits	Read/ Write	Value (Default)	Comment
Vender ID	00h	15 : 0	R	1033h	NEC's vendor ID
Device ID	02h	15 : 0	R	0035h	NEC OHCI's device ID
Command	04h	15 : 0			See **Table 4-14.**
Status	06h	15 : 0			See **Table 4-15.**
Revision ID	08h	7 : 0	R	43h	Revision ID
Class Code -Base Class	09h	23 : 16	R	0Ch	Serial Bus Controller Device
-Sub_Class		15 : 8	R	03h	USB Device
-Programming Interface		7 : 0	R	10h	Open HCI Host Controller
Cache Line Size	0Ch	7 : 0	R/W	00h	Cache Line Size
Latency Timer	0Dh	7 : 2	R/W	000010b	Latency Timer for this PCI bus master [Note]
		1 : 0	R	00b	
Header Type	0Eh	7 : 0	R	00h	Not a PCI-to-PCI Bridge
BIST	0Fh	7 : 0	R	00h	BIST is not supported.
Base Address Register	10h	31 : 0			See **Table 4-16.**
Subsystem Vender ID	2Ch	15 : 0	R (/W)	1033h	Indicates Subsystem Vender ID
Subsystem ID	2Eh	15 : 0	R (/W)	0035h	Indicates Subsystem ID
Expansion ROM Base Address	30h	31 : 0	R	0000h	Expansion ROM address
Cap_ptr	34h	7 : 0	R	40h	Indicates Capability List header
Interrupt Line	3Ch	7 : 0	R/W	00h	Indicates interrupt line's route
Interrupt Pin	3Dh	7 : 0	R	02h	Routing to INTB0
Min_Gnt	3Eh	7 : 0	R (/W)	01h	Minimum request for burst period.
Max_Lat	3Fh	7 : 0	R (/W)	2Ah	Frequency request of PCI access
Cap_ID	40h	7 : 0	R	01h	ID for PCI Power Management reg.
Next_Item_Ptr	41h	7 : 0	R	00h	There is no next item in the list.
PMC	42h	15 : 0			See **Table 4-17.**
PMCSR	44h	15 : 0			See **Table 4-18.**
PMCSR_BSE	46h	7 : 0	R	00h	Not PCI-to-PCI bridge device
Data	47h	7 : 0	R	00h	No support

Note This register should be set by system (OS). However, some system may not set this register. So, default value of this register is 08h.

Remark The register marked as "(/W)" in the above table can be written by BIOS when ID_Write_Enable bit is set to "1". On the other, the value of these registers can be loaded from external serial ROM with I^{2}C I/F before starting PCI configuration registers access if serial ROM is available.

Table 4-14. Command Register

Field	bit	Read/Write	Value (Default)	Comment
I/O space	0	R	0b	No support I/O space.
Memory space	1	R/W	0b	Controls response to memory access 0: Memory access disable 1: Memory access enable After reset, this bit is set to "0".
Bus Master	2	R/W	0b	Controls bus master operation 0: Bus master functionality disable 1: Bus master functionality enable After reset, this bit is set to "0".
Special Cycles	3	R	0b	Ignores special cycles
Memory write and invalidate enable	4	R/W	0b	Enables memory write and invalidate command. 0: Memory write and invalidate command disable 1: Memory write and invalidate command enable After reset, this bit is set to "0".
VGA palette snoop	5	R	0b	Sets VGA palette snoop as invalid
Parity Error response	6	R/W	0b	Controls response to parity error. 0: PERR0 can not assert. 1: PERR0 can assert. Even this bit is set to "0", when parity error is detected, Detected parity error bit in Status Reg. is set to "1". After reset, this bit is set to "0".
Wait cycle control	7	R	0b	Address/data stepping is not supported.
SERR# enable	8	R/W	0b	Controls response to system errors. 0: SERR0 can not assert. 1: SERR0 can assert. After reset, this bit is set to "0".
Fast back-to-back enable	9	R	0b	Fast back-to-back access is not supported.
Reserved	15 : 10	R	000000b	Reserved

Table 4-15. Status Register

Field	bit	Read/ Write	Value	Comment
Reserved	3 : 0	R	0000b	Reserved
Capabilities List	4	R	1b	Supports Power Management
66 MHz capable	5	R	0b	33-MHz operation
Reserved	6	R	0b	Reserved
Fast back-to-back capable	7	R	0b	Fast back-to-back access is not supported.
Data Parity Error detected	8	R/W		"High" is set to this bit when the following three conditions are met. (1) PERR0 is asserted by the parity error or assertion of PERR0 was detected. (2) The parity error source was the bus master during the bus cycle in which the parity error occurred. (3) "High" has been set to the command register's Parity Error response bit. This bit can be cleared by set to "1" from PCI.
DEVSEL timing	10 : 9	R	01b	DEVSEL0 assert timing: Medium speed
Signaled target abort	11	R/W		The target sets to "1" whenever it terminates a transaction with Target-abort. This bit can be cleared by set to "1" from PCI.
Received target abort	12	R/W		The master sets to "1" whenever its transaction is terminated with Target-abort. This bit can be cleared by set to"1" from PCI.
Received master abort	13	R/W		The master sets to "1" whenever it terminates a transaction with Master-abort. This bit can be cleared by set to "1" from PCI.
Signaled system error	14	R/W		"High" is set to this bit when SERR0 is asserted. This bit can be cleared by set to "1" from PCI.
Detected parity error	15	R/W		"High" is set to this bit when Address/Data parity error is detected even Parity Error response bit in Command Reg. is set to "0". This bit can be cleared by set to "1" from PCI.

Table 4-16. Base Address (BAR_OHCI) Register

Field	bit	Read/ Write	Value (Default)	Comment
Memory space indicator	0	R	0b	Operational registers are mapped to main memory space.
Type	2 : 1	R	00b	Operational registers can be allocated in any part of the 4-G main memory space.
Prefetchable	3	R	0b	Prefetch is disabled.
Base address (LSB)	11 : 4	R	00h	Operational registers have a 4-Kbyte address space.
Base address (MSB)	31 : 12	R/W	000h	Indicates the high-order 20 bits of the base address in the Operational registers.

Table 4-17. Power Management Capabilities (PMC) Register

Field	bit	Read/ Write	Value (Default)	Comment
Version	2 : 0	R	010b	PCI Power Management Interface Specification release 1.1
PME Clock	3	R	0b	PCLK is not required for PME0 assertion.
Reserved	4	R	0b	Reserved
DSI	5	R	0b	Does not required Specific Initialization before the generic class device driver is able to use it.
Aux_Current	8 : 6	R (/W)	000b	Indicates current requirement If PME0 generation from D3$_{cold}$ is not supported by this host controller core, this field must return a value of "000b" when read. If PME0 generation from D3$_{cold}$ is supported by this host controller core, following assignments apply: Bit 3.3Vaux 8 7 6 Max. Current Required 1 1 1 375 mA 1 1 0 320 mA 1 0 1 270 mA 1 0 0 220 mA 0 1 1 160 mA 0 1 0 100 mA 0 0 1 55 mA 0 0 0 0 (self powerd)
D1_support	9	R	1b	Support D1 Power Management State
D2_support	10	R	1b	Support D2 Power Management State
PME_support	15	R (/W)	0b	Indicates whether D3$_{cold}$ is supported or not.
	14 : 11	R	1111b	PME0 can be asserted from D0, D1, D2, D3$_{hot}$.

Remark The register marked as "(/W)" in the above table can be written by BIOS when ID_Write_Enable bit is set to "1". On the other, the value of these registers can be loaded from external serial ROM with I^{2}C I/F before starting PCI configuration registers access if serial ROM is available.

Table 4-18. Power Management Control/Status (PMCSR) Register

Field	bit	Read/ Write	Value (Default)	Comment
Power State	1 : 0	R/W	00b	Shows power state of a host controller core and sets the host controller core into a new power state. 00b: D0 01b: D1 10b: D2 11b: D3$_{hot}$
Reserved	7 : 2	R	00h	Reserved
PME_En	8	R/W	0b	Enable to assert PME0. 0: PME0 assertion disable 1: PME0 assertion enable This bit default to "0" if the host controller core does not support PME0 generation from D3$_{cold}$. If the host controller core supports PME0 generation from D3$_{cold}$, then this bit is sticky and must be explicitly cleared by the OS each time it is initially loaded.
Data_Select	12 : 9	R	0000b	Data register is not implemented.
Data_Scale	14 : 13	R	00b	Data register is not implemented.
PME_Status	15	R/W	0b	PME_Status is set to "1" when ResumeDetected (RD) bit of HcInterruptStatus Reg. in OHCI is set to "1" even PME_En bit is set to "0". This bit can be cleared by set to "1" from PCI. This bit default to "0" if the host controller core does not support PME0 generation from D3$_{cold}$. If the host controller core supports PME0 generation from D3$_{cold}$, then this bit is sticky and must be explicitly cleared by the OS each time it is initially loaded.

Remark When Power State is not "D0", the function assumes that it is in Global Suspend and internal clock is stopped.

4.1.3 PCI configuration space for EHCI host controller

Table 4-19. Configuration Space for EHCI Host Controller

31 24	23 16	15 8	7 0	Offset
Device ID		Vender ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
USB Base Address Register				10h
Reserved				14h
^				18h
^				1Ch
^				20h
^				24h
Reserved				28h
Subsystem ID		Subsystem Vender ID		2Ch
Expansion ROM Base Address				30h
Reserved			Cap_ptr	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
PMC		Next_Item_Ptr	Cap_ID	40h
Data	PMCSR_BSE	PMCSR		44h
Reserved				46h
^				….
^				5Ch
PORTWAKECAP		FLADJ	SBRN	60h
Reserved				64h
^				….
^				DCh
EXT1				E0h
EXT2				E4h
USBLEGSUP				E8h
USBLEGCTLSTS				ECh

Table 4-20. Register Information

(1/2)

Register	Address	bits	Read/Write	Value (Default)	Comment
Vender ID	00h	15 : 0	R	1033h	NEC's vendor ID
Device ID	02h	15 : 0	R	00E0h	NEC EHCI's device ID
Command	04h	15 : 0		See **Table 4-21.**	
Status	06h	15 : 0		See **Table 4-22.**	
Revision ID	08h	7 : 0	R	04h	Version 1.0
Class Code -Base Class	09h	23 : 16	R	0Ch	Serial Bus Controller Device
-Sub_Class		15 : 8	R	03h	USB Device
-Programming Interface		7 : 0	R	20h	Enhanced HCI Host Controller
Cache Line Size	0Ch	7 : 0	R/W	00h	Cache Line Size
Latency Timer	0Dh	7 : 2	R/W	010001b	Latency Timer for this PCI bus master **Note**
		1 : 0	R	00b	
Header Type	0Eh	7 : 0	R	00h	Not a PCI-to-PCI Bridge.
BIST	0Fh	7 : 0	R	00h	BIST is not supported.
Base Address Register	10h	31 : 0		See **Table 4-23.**	
Subsystem Vender ID	2Ch	15 : 0	R (/W)	1033h	Indicates Subsystem Vender ID
Subsystem ID	2Eh	15 : 0	R (/W)	00E0h	Indicates Subsystem ID
Expansion ROM Base Address	30h	31 : 0	R	0000h	Expansion ROM address
Cap_ptr	34h	7 : 0	R	40h	Indicates Capability List header
Interrupt Line	3Ch	7 : 0	R/W	00h	Indicates interrupt line's route
Interrupt Pin	3Dh	7 : 0	R	03h	Routing to INTC0
Min_Gnt	3Eh	7 : 0	R (/W)	10h	Minimum request for burst period.
Max_Lat	3Fh	7 : 0	R (/W)	22h	Frequency request of PCI access
Cap_ID	40h	7 : 0	R	01h	ID for PCI Power Management reg.
Next_Item_Ptr	41h	7 : 0	R	00h	There is no next item in the list.
PMC	42h	15 : 0		See **Table 4-24.**	
PMCSR	44h	15 : 0		See **Table 4-25.**	
PMCSR_BSE	46h	7 : 0	R	00h	Not PCI-to-PCI bridge device
Data	47h	7 : 0	R	00h	No support
SBRN	60h	7 : 0	R	20h	Serial Bus Release Number
FLADJ	61h	5 : 0	R/W	20h	Frame Length Adjustment
		7 : 6	R	00b	Default SOF cycle time is 60000.
PORTWAKECAP	62h	15 : 0	R/W	003Fh	Port wake capabilities (1:5) ports are to be used for wake events.

Note This register should be set by system (OS). However, some system may not set this register. So, default value of this register is 44h.

(2/2)

Register	Address	bits	Read/Write	Value (Default)	Comment
EXT1	E0h	32 : 0			See **Table 4-26.**
EXT2	E4h	32 : 0			See **Table 4-27.**
USBLEGSUP	E8h	32 : 0	R, R/W	00000001h	USB Legacy Support Extended Capability
USBLEGCTLSTS	ECh	32 : 0	R, R/W, R/W/C	0000h	USB Legacy Support Control/Status

Remark The register marked as "(/W)" in the above table can be written by BIOS when ID_Write_Enable bit is set to "1". On the other, the value of these registers can be loaded from external serial ROM with I^{2}C I/F before starting PCI configuration registers access if serial ROM is available.

Table 4-21. Command Register

Field	bit	Read/ Write	Value (Default)	Comment
I/O space	0	R	0b	No support I/O space.
Memory space	1	R/W	0b	Controls response to memory access 0: Memory access disable 1: Memory access enable After reset, this bit is set to "0".
Bus Master	2	R/W	0b	Controls bus master operation 0: Bus master functionality disable 1: Bus master functionality enable After reset, this bit is set to "0".
Special Cycles	3	R	0b	Ignores special cycles
Memory write and invalidate enable	4	R/W	0b	Enables memory write and invalidate command. 0: Memory write and invalidate command disable 1: Memory write and invalidate command enable After reset, this bit is set to "0".
VGA palette snoop	5	R	0b	Sets VGA palette snoop as invalid
Parity Error response	6	R/W	0b	Controls response to parity error. 0: PERR0 can not assert. 1: PERR0 can assert. Even this bit is set to "0", when parity error is detected, Detected parity error bit in Status Reg. is set to "1". After reset, this bit is set to "0".
Wait cycle control	7	R	0b	Address/data stepping is not supported.
SERR# enable	8	R/W	0b	Controls response to system errors. 0: SERR0 can not assert. 1: SERR0 can assert. After reset, this bit is set to "0".
Fast back-to-back enable	9	R	0b	Fast back-to-back access is not supported.
Reserved	15 : 10	R	000000b	Reserved

Table 4-22. Status Register

Field	bit	Read/Write	Value	Comment
Reserved	3 : 0	R	0000b	Reserved
Capabilities List	4	R	1b	Supports Power Management
66 MHz capable	5	R	0b	33-MHz operation
Reserved	6	R	0b	Reserved
Fast back-to-back capable	7	R	0b	Fast back-to-back access is not supported.
Data Parity Error detected	8	R/W		"High" is set to this bit when the following three conditions are met. (1) PERR0 is asserted by the parity error or assertion of PERR0 was detected. (2) The parity error source was the bus master during the bus cycle in which the parity error occurred. (3) "High" has been set to the command register's Parity Error response bit. This bit can be cleared by set to "1" from PCI.
DEVSEL timing	10 : 9	R	01b	DEVSEL0 assert timing: Medium speed
Signaled target abort	11	R/W		The target set to "1" whenever it terminates a transaction with Target-abort. This bit can be cleared by set to "1" from PCI.
Received target abort	12	R/W		The master set to "1" whenever its transaction is terminated with Target-abort. This bit can be cleared by set to "1" from PCI.
Received master abort	13	R/W		The master set to "1" whenever it terminates a transaction with Master-abort. This bit can be cleared by set to "1" from PCI.
Signaled system error	14	R/W		"High" is set to this bit when SERR0 is asserted. This bit can be cleared by set to "1" from PCI.
Detected parity error	15	R/W		"High" is set to this bit when Address/Data parity error is detected even Parity Error response bit in Command Reg. is set to "0". This bit can be cleared by set to "1" from PCI.

Table 4-23. Base Address Register

Field	bit	Read/Write	Value (Default)	Comment
Memory space indicator	0	R	0b	EHCI registers are mapped to main memory space.
Type	2 : 1	R	00b	Capability and Operational registers can be mapped into 32-bit addressing space.
Prefetchable	3	R	0b	Prefetch is disabled.
Base address (LSB)	7 : 4	R	00h	EHCI registers have a 256 byte address space.
Base address (MSB)	31 : 8	R/W	000h	Indicates the high-order 24 bits of the base address in the Operational registers.

Table 4-24. Power Management Capabilities (PMC) Register

Field	bit	Read/Write	Value (Default)	Comment
Version	2 : 0	R	010b	PCI Power Management Interface Specification release 1.1
PME Clock	3	R	0b	PCLK is not required for PME0 assertion.
Reserved	4	R	0b	Reserved
DSI	5	R	0b	Does not required Specific Initialization before the generic class device driver is able to use it.
Aux_Current	8 : 6	R (/W)	000b	Indicates current requirement If PME0 generation from $D3_{cold}$ is not supported by this host controller core, this field must return a value of "000b" when read If PME0 generation from $D3_{cold}$ is supported by this host controller core, following assignments apply: Bit 3.3Vaux 8 7 6 Max. Current Required 1 1 1 375 mA 1 1 0 320 mA 1 0 1 270 mA 1 0 0 220 mA 0 1 1 160 mA 0 1 0 100 mA 0 0 1 55 mA 0 0 0 0 (self powerd)
D1_support	9	R	1b	Support D1 Power Management State
D2_support	10	R	1b	Support D2 Power Management State
PME_support	15	R (/W)	0b	Indicates whether $D3_{cold}$ is supported or not.
	14 : 11	R	1111b	PME0 can be asserted from D0, D1, D2, $D3_{hot}$.

Remark The register marked as "(/W)" in the above table can be written by BIOS when ID_Write_Enable bit is set to "1". On the other, the value of these registers can be loaded from external serial ROM with I^2C I/F before starting PCI configuration registers access if serial ROM is available.

Table 4-25. Power Management Control/Status (PMCSR) Register

Field	bit	Read/ Write	Value (Default)	Comment
Power State	1 : 0	R/W	00b	Shows power state of a host controller core and sets the host controller core into a new power state. 00b: D0 01b: D1 10b: D2 11b: D3$_{hot}$
Reserved	7 : 2	R	00h	Reserved
PME_En	8	R/W	0b	Enable to assert PME0. 0: PME0 assertion disable 1: PME0 assertion enable This bit default to "0" if the host controller core does not support PME0 generation from D3$_{cold}$. If the host controller core supports PME0 generation from D3$_{cold}$, then this bit is sticky and must be explicitly cleared by the OS each time it is initially loaded.
Data_Select	12 : 9	R	0000b	Data register is not implemented.
Data_Scale	14 : 13	R	00b	Data register is not implemented.
PME_Status	15	R/W	0b	PME_Status is set to "1" when event, which is allowed by PORTSC Reg. in EHCI, is occurred even PME_En bit is set to "0". This bit can be cleared by set to "1" from PCI. This bit default to "0" if the host controller core does not support PME0 generation from D3$_{cold}$. If the host controller core supports PME0 generation from D3$_{cold}$, then this bit is sticky and must be explicitly cleared by the OS each time it is initially loaded.

Remark When Power State is not "D0", the function assumes that it is in Global Suspend and internal clock is stopped.

Table 4-26. EXT1 Register

Field	bit	Read/Write	Value (Default)	Comment
Port No	2 : 0	R/W	5h	Configures valid port number. Value Active ports 5h Port 1, 2, 3, 4, and 5 4h Port 1, 2, 3, and 4 3h Port 1, 2, and 3 2h Port 1 and 2 Prohibited setting besides above value.
Legc_mode	3	R/W	0b	Controls the decoding for I/O access to 60h/64h. 0: The HC intercepts 60h/64h access without PCI I/O address space. 1: The HC intercepts 60h/64h access using PCI I/O address space which is indicated in I/O address register of OHCI #1's configuration space. When "LEGC" pin is "low", the setting of this bit is ignored.
NEC private #1	4	R/W	0b	Prohibited setting to "1".
NEC private #2	5	R/W	0b	Prohibited setting to "1".
NEC private #3	6	R/W	0b	Prohibited setting to "1".
ID_Wirte_Enable	7	R/W	0b	Write protection of Subsystem ID and Subsystem Vendor ID, etc. 0: Write Mask 1: Write Enable
NEC private #4	11 : 8	R/W	3h	Prohibited setting the value except for "3h".
NEC private #5	15 : 12	R/W	3h	Prohibited setting the value except for "3h".
NEC private #6	20 :16	R/W	10h	Prohibited setting the value except for "10h"

PPC_setting	21	R/W	1b	Set PPC bit in HCSPARAMS reg.
				
				0: PPC is set to a zero.
				   HC does not have the port power control switches. And then, port power is always active.
				
				1: PPC is set to a one.
				   HC has the port power control switches.
				
				If port power is always active, this bit should be set to a zero and NPS bit in OHCI's HcRhDescriptorA reg. should be set to a one.

NEC private #7	22	R/W	0b	Prohibited setting to "1".
NEC private #9	23	R	1b	
NEC private #8	31 : 24	R/W	6Ch	Prohibited setting the value except for "6Ch"

Remarks 1. The value of these registers except for ID_Wirte_Enable bit can be loaded from external serial ROM with I²C I/F before starting PCI configuration registers access if serial ROM is available.

2. This register equals to EXT1 register which is indicated in OHCI #1 configuration space. So, this register can be accessed by offset address E0h of OHCI #1 configuration register.

Table 4-27. EXT2 Register

Field	bit	Read/ Write	Value (Default)	Comment
Reserved	0	R	0b	Reserved
NEC private #10	4:1	R/W	0h	Prohibited setting the value except for "0h".
Clock_ sel	5	R/W	0b	0: System clock is 30-MHz X'tal. 1: System clock is 48-MHz Oscillator.
NEC private #11	6	R/W	0b	Prohibited setting to "1".
Reserved	31 : 7	R	000h	Reserved

Remark This register equals to EXT2 register which indicated in OHCI #1 configuration space. So, this register bit can be accessed by offset address Eh4 of OHCI #1 configuration register.

4.2 OHCI Operational Registers

The OHCI Host controller includes the Operational Registers, which are the starting point for communication with the host CPU. The PCI Configuration Space's Base Address (BAR_OHCI) Register in OHCI Host Controllers indicates the base address of Operational Registers. This set of registers is mapped to a 4-Kbyte range in the 4-Gbyte main memory space, where it is used by the HCD (Host Controller Driver). All of the registers should be read and written as Dwords. For a more detailed description, see the **Open HCI Specification Release 1.0a** and **OpenHCI Legacy Support Interface Specification Release Version 1.01**.

Figure 4-1. OpenHCI's PCI Configuration Space

4.2.1 Mapping of operational registers for OHCI host controller #1

Table 4-28. Operational Registers for OHCI Host Controller #1

31	0	Offset
HcRevision		00h
HcControl		04h
HcCommandStatus		08h
HcInterruptStatus		0Ch
HcInterruptEnable		10h
HcInterruptDisable		14h
HcHCCA		18h
HcPeriodCurrentED		1Ch
HcControlHeadED		20h
HcControlCurrentED		24h
HcBulkHeadED		28h
HcBulkCurrentED		2Ch
HcDoneHead		30h
HcFmInterval		34h
HcFmRemaining		38h
HcFmNumber		3Ch
HcPeriodicStart		40h
HcLSThreshold		44h
HcRhDescriptorA		48h
HcRhDescriptorB		4Ch
HcRhStatus		50h
HcRhPortStatus1		54h
HcRhPortStatus2		58h
HcRhPortStatus3		5Ch

Table 4-29. Legacy Support Registers for OHCI Host Controller #1

31	0	Memory Offset	I/O Address
HceControl		100h	
HceInput		104h	60h/64h
HceOutput		108h	60h
HceStatus		10Ch	64h

4.2.2 Mapping of operational registers for OHCI host controller #2

Table 4-30. Operational Registers for OHCI Host Controller #2

31 0	Offset
HcRevision	00h
HcControl	04h
HcCommandStatus	08h
HcInterruptStatus	0Ch
HcInterruptEnable	10h
HcInterruptDisable	14h
HcHCCA	18h
HcPeriodCurrentED	1Ch
HcControlHeadED	20h
HcControlCurrentED	24h
HcBulkHeadED	28h
HcBulkCurrentED	2Ch
HcDoneHead	30h
HcFmInterval	34h
HcFmRemaining	38h
HcFmNumber	3Ch
HcPeriodicStart	40h
HcLSThreshold	44h
HcRhDescriptorA	48h
HcRhDescriptorB	4Ch
HcRhStatus	50h
HcRhPortStatus1	54h
HcRhPortStatus2	58h

4.2.3 Overview of OHCI operational registers

Unless specifically stated otherwise, the meaning and value of each register for OHCI Host Controller #2 equals to that of OHCI Host Controller #1.

Register: HcRevision   **Offset Address: 00h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
Revision	7 : 0	R	R	10h	Complies with OpenHCI R1.0
Legacy	8	R	R/W	Xb	Includes a legacy support register. It is set to suit the setting of external pin "LEGC". LEGC = 0 → Set to "0" LEGC = 1 → Set to "1"
Reserved	31 : 9	R	R	0h	Reserved

Remark   The address space for Legacy Function Controller is allocated in the address space of OHCI Host Controller #1. There is no Legacy Function Controller to access in OHCI Host Controller #2 address space. However, Legacy Function controller, which is allocated in the address space of OHCI Host Controller #1, should handle to emulate Legacy (PS/2) keyboard and mouse functionality by USB keyboard and mouse which is connected to any ports. So, BIOS must handle this operating. And then OHCI Host Controller #2 supports "Legacy" bit even if Legacy Function Controller is not allocated in OHCI Host Controller #2 address space.

Register: HcControl　　　　　　**Offset Address: 04h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
ControlBulkServiceRatio (CBSR)	1 : 0	R/W	R	00b	Indicates the service ratio between Control and Bulk EDs. <table><tr><td>CBSR</td><td>No. of Control EDs Over Bulk EDs Served</td></tr><tr><td>0</td><td>1 : 1</td></tr><tr><td>1</td><td>2 : 1</td></tr><tr><td>2</td><td>3 : 1</td></tr><tr><td>3</td><td>4 : 1</td></tr></table>
PeriodicListEnable (PLE)	2	R/W	R	0b	Sets the next frame's periodic list servicing as valid or invalid. 1: Valid, 0: Invalid
IsochronousEnable (IE)	3	R/W	R	0b	Sets the next frame's isochronous ED servicing as valid or invalid. 1: Valid, 0: Invalid
ControlListEnable (CLE)	4	R/W	R	0b	Sets the next frame's control list servicing as valid or invalid. 1: Valid, 0: Invalid
BulkListEnable (BLE)	5	R/W	R	0b	Sets the next frame's bulk list servicing as valid or invalid. 1: Valid, 0: Invalid
HostControllerFunctional StateforUSB (HCFS)	7 : 6	R/W	R/W	00b (H/W_R) 11b (S/W_R)	00b: USBRESET 01b: USBRESUME 10b: USBOPERATIONAL 11b: USBSUSPEND
InterruptRouting (IR)[Note]	8	R/W	R	0b	This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. 1: SMI0 output, 0: INTx0 output
RemoteWakeup Connected (RWC)[Note]	9	R/W	R/W	0b	This bit indicates whether HC support remote wakeup signaling. If remote wakeup is supported and used by system, it will be the responsibility of system firmware to set this bit during POST.
RemoteWakeupEnable (RWE)	10	R/W	R	0b	This bit control PME0 assertion. If this bit is set to "high", when ResumeDetected bit is set, PME0 will be asserted. 1: PME0 enable, 0: PME0 disable
Reserved	31 : 11	R	R	0h	Reserved

Note Only Hardware Reset is available.

Remarks 1. H/W_R = Hardware Reset
2. S/W_R = Software Reset

Register: HcCommandStatus   **Offset Address: 08h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
HostControllerReset (HCR)	0	R/W	R/W	0b	HC software reset. This bit is set by the HCD and cleared by the HC.
ControlListFilled (CLF)	1	R/W	R/W	0b	Indicates whether any TDs exist on the control list or not.
BulkListFilled (BLF)	2	R/W	R/W	0b	Indicates whether any TDs exist on the bulk list or not.
OwnershipChangeRequest (OCR)	3	R/W	R/W	0b	This bit is set by the HCD to request a change of control of the HC.
Reserved	15 : 4	R	R	0h	Reserved
SchedulingOverrunCount (SOC)	17 : 16	R	R/W	00b	These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b.
Reserved	31 : 18	R	R	0h	Reserved

Register: HcInterruptStatus   **Offset Address: 0Ch**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
SchedulingOverrun (SO)	0	R/W	R/W	0b	This bit is set when the USB schedule for the current frame overruns.
WritebackDoneHead (WDH)	1	R/W	R/W	0b	This bit is set when HC has written HcDoneHead to HccaDoneHead. The HCD should only clear this bit after it has saved the contents of HccaDoneHead.
StartofFrame (SF)	2	R/W	R/W	0b	This bit is set at each start of a frame.
ResumeDetected (RD)	3	R/W	R/W	0b	This bit is set when a resume signal has been detected. This bit is not set when HCD sets the USBRESUME state.
UnrecoverableError (UE)	4	R/W	R/W	0b	This bit is set when a system error that is not related to USB has been detected.
FrameNumberOverflow (FNO)	5	R/W	R/W	0b	This bit is set when the MSb (bit 15) of HcFmNumber has changed its value, from "0" to "1" or from "1" to "0".
RootHubStatusChange (RHSC)	6	R/W	R/W	0b	This bit is set when the content of either HcRhStatus or HcRhPortStatusX has changed.
Reserved	29 : 7	R	R	0h	Reserved
OwnershipChange (OC)	30	R/W	R/W	0b	This bit is set by the HC when the HCD has set the OCR field in the HcCommandStatus register. If this event is not masked, it immediately generates a system management interrupt (SMI0) even if IR bit is set to "0".
Other	31	R	R	0b	

Remark HCD will clear specific bits in this register by writing "1" to bit positions to be cleared.

Register: HcInterruptEnable   **Offset Address: 10h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
SO	0	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Scheduling Overrun
WDH	1	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Writeback HcDoneHead
SF	2	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Start of Frame
RD	3	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Resume Detect
UE	4	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Unrecoverable Error
FNO	5	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Frame Number Overflow
RHSC	6	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Root Hub Status Change
Reserved	29 : 7	R	R	0h	Reserved
OC	30	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Ownership Change
Master Interrupt Enable (MIE)	31	R/W	R	0b	0: Ignore 1: Interrupt triggering is enabled when an event other than those listed above occurs.

Register: HcInterruptDisable   **Offset Address: 14h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HC		
SO	0	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Scheduling Overrun
WDH	1	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Writeback HcDoneHead
SF	2	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Start of Frame
RD	3	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Resume Detect
UE	4	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Unrecoverable Error
FNO	5	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Frame Number Overflow
RHSC	6	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Root Hub Status Change
Reserved	29 : 7	R	R	0h	Reserved
OC	30	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Ownership Change
Master Interrupt Enable (MIE)	31	R/W	R	0b	0: Ignore 1: Interrupt triggering is disabled when an event other than those listed above occurs.

Register: HcHCCA   **Offset Address: 18h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HC		
Host Controller Communication Area (HCCA)	7 : 0	R	R	00h	This is the base address of the Host Controller Communication Area. Since it is allocated in 256-byte boundary, the bits 0 through 7are fixed at "0".
	31 : 8	R/W	R	0h	

Register: HcPeriodCurrentED   **Offset Address: 1Ch**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HC		
PeriodCurrentED (PCED)	3 : 0	R	R	00h	This is the physical address of the current Isochronous or Interrupt ED in the periodic list being serviced during the current frame. Since the ED is allocated in 16-byte boundary, bits 0 through 4 are fixed at "0".
	31 : 4	R	R/W	0h	

Register: HcControlHeadED   **Offset Address: 20h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
ControlHeadED (CHED)	3 : 0	R	R	00h	This is the physical address of the first ED of the control list. In case of setting this pointer to Null, it must wait 1 frame after ControlListEnable is cleared.
	31 : 4	R/W	R	0h	

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Register: HcControlCurrentED   **Offset Address: 24h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
ControlCurrentED (CCED)	3 : 0	R	R	00h	This is the physical address of the current ED of the control list.
	31 : 4	R/W	R/W	0h	

Register: HcBulkHeadED   **Offset Address: 28h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
BulkHeadED (BHED)	3 : 0	R	R	00h	This is the physical address of the first ED of the bulk list. In case of setting this pointer to Null, it must wait 1 frame after BulkListEnable is cleared.
	31 : 4	R/W	R	0h	

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Register: HcBulkCurrentED   **Offset Address: 2Ch**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
BulkCurrentED (BCED)	3 : 0	R	R	00h	This is the physical address of the current ED of the bulk list.
	31 : 4	R/W	R/W	0h	

Register: HcDoneHead   **Offset Address: 30h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
DoneHead (DH)	3 : 0	R	R	00h	This is the physical address of the last completed TD to be added to the Done queue.
	31 : 4	R	R/W	0h	

Register: HcFmInterval   **Offset Address: 34h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
FrameInterval (FI)	13 : 0	R/W	R	2EDFh	This bit indicates a bit time value between two consecutive SOFs.
Reserved	15 : 14	R	R	0h	Reserved
FSLargestDataPacket (FSMPS)	30 : 16	R/W	R	0000h	This is the maximum number of data bits that can be sent or received in one transaction.
FrameIntervalToggle (FIT)	31	R/W	R	0b	This is inverted when loading new value to FI.

Register: HcFmRemaining   **Offset Address: 38h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
FrameRemaining (FR)	13 : 0	R	R/W	2EDFh	This is a 14-bit down counter which indicates the remaining bit time in the current frame.
Reserved	30 : 14	R	R	0h	Reserved
FrameRemainingToggle (FRT)	31	R	R/W	0b	When the value of FR becomes "0", a value is loaded from the FIT field of the HcFmInterval register.

Register: HcFmNumber   **Offset Address: 3Ch**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
FrameNumber (FN)	15 : 0	R	R/W	0h	This is a 16-bit counter that is incremented when HcFmRemaining is reloaded.
Reserved	31 : 16	R	R	0h	Reserved

Register: HcPeriodicStart   **Offset Address: 40h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
PeriodicStart (PS)	13 : 0	R/W	R	0h	This indicates that periodic list servicing should be started.
Reserved	31 : 14	R	R	0h	Reserved

Register: HcLSThreshold   **Offset Address: 44h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
LSThreshold (LST)	11 : 0	R/W	R	0628h	This includes a value that is used to determine whether or not to send the LS packet before the EOF.
Reserved	31 : 12	R	R	0h	Reserved

Register: HcRhDescriptorA   **Offset Address: 48h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
NumberDownstreamPorts (NDP)[Note 1]	7 : 0	R	R	**Note2**	These bits indicate the number of downstream ports supported by the root hub.
PowerSwitchingMode (PSM)[Note 1]	8	R/W	R	1b	0: Power supply is applied to all ports at the same time. 1: Power supply is applied separately to each port.
NoPowerSwitching (NPS)[Note 1]	9	R/W	R	0b	0: Power supply to ports can be switched on and off. 1: Power supply to ports is always applied when HC is powered on.
DeviceType (DT)[Note 1]	10	R	R	0b	Indicates that the root hub is not a compound device.
OverCurrentProtection Mode (OCPM)[Note 1]	11	R/W	R	1b	0: Overcurrent status is reported for all downstream ports at once. 1: Overcurrent status is reported separately for each port.
NoOverCurrentProtection (NOCP)[Note 1]	12	R/W	R	0b	0: Overcurrent status is reported. 1: Overcurrent protection is not supported.
Reserved	23 : 13	R	R	0h	Reserved
PowerOnToPowerGood Time (POTPGT)[Note 1]	31 : 24	R/W	R	0Fh	These bits indicate the amount of time that the HCD must wait before accessing the root hub port to which a power supply is applied.

Notes **1.** These fields can only be reset by hardware reset.

2. These bits are set by the value of Port No field in PCI configuration's EXT1 register as wing table.

Table 4-31. Port No Field vs NDP Field

Port No	OHCI #1	OHCI #2
	NDP	NDP
5	3h	2h
4	2h	2h
3	2h	1h
2	1h	1h

Register: HcRhDescriptorB   **Offset Address: 4Ch**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
DeviceRemovable (DR) Note 1	3 : 0	R/W	R	**Note 2, 3**	bit0: Reserved bit1: Device is connected to Port#1 bit2: Device is connected to Port#2 bit3: Device is connected to Port#3
Reserved	15 : 4	R	R	0h	Reserved
PortPowerControlMask (PPCM) Note 1	19 : 16	R/W	R	**Note 3**	bit0: Reserved bit1: Power supply to Port#1 is masked bit2: Power supply to Port#2 is masked bit3: Power supply to Port#3 is masked
Reserved	31 : 20	R	R	0h	Reserved

Notes 1. These fields can only be reset by hardware reset.

    2. These bits should be set to 0000h to support EHCI host controller.

    3. These bits are set by the value of Port No field in PCI configuration's EXT1 register as following table.

Table 4-32. Port No Field vs DR and PPCM Field

Port No	OHCI #1								OHCI #2							
	bit19	bit18	bit17	bit16	bit3	bit2	bit1	bit0	bit19	bit18	bit17	bit16	bit3	bit2	bit1	bit0
5	PPCM (Eh)				DR (0h)				R	PPCM (6h)			R	DR (0h)		
4	R	PPCM (6h)			R	DR (0h)			R	PPCM (6h)			R	DR (0h)		
3	R	PPCM (6h)			R	DR (0h)			R	PPCM (2h)			R	DR (0h)		
2	R		PPCM (2h)		R		DR (0h)		R	PPCM (2h)			R	DR (0h)		

The numbers in () represent the default value for each field. "**R**" indicates "reserved" field. Reserved bit is read-only bit and it is set to zero.

Register: HcRhStatus   **Offset Address: 50h**

Field	Bit	Read/Write		Value	Comment
		HCD	HC	(Default)	
LocalPowerStatus (LPS) ^{Note}	0	R	R	0b	The root hub does not support local power status.
ClearGlobalPower (CGP) ^{Note}		W	R	0b	1: Power supply to all ports is off when PSM = 0. When PSM = 1, only PPS is cleared for ports whose PPCM has not been set. 0: No change
OverCurrentIndicator (OCI)^{Note}	1	R	R/W	0b	The following occurs when overcurrent status is reported to all downstream ports at once. 1: Overcurrent status exists 0: Normal power supply operations Be sure that this is set to "0" when overcurrent status is reported for each port.
Reserved	14 : 2	R	R	0h	Reserved
DeviceRemoteWakeup Enable (DRWE) ^{Note}	15	R	R	0b	0: CSC is not a remote wakeup event 1: CSC is a remote wakeup event
SetRemoteWakeupEnable (SRWE) ^{Note}		W	R	0b	1: Sets DRWE 0: No change
LocalPowerStatusChange (LPSC) ^{Note}	16	R	R	0b	The root hub does not support local power status.
SetGlobalPower (SGP) ^{Note}		W	R	0b	1: Power supply to all ports is on when PSM = 0. When PSM = 1, only PPS is set for ports whose PPCM has not been set. 0: No change
OverCurrentIndicator Change (OCIC) ^{Note}	17	R/W	R/W	0b	HC sets "1" when a change has occurred in OCI. It is cleared when the HCD writes "1". There is no change when the HCD writes "0".
Reserved	30 : 18	R	R	0h	Reserved
ClearRemoteWakeup Enable (CRWE) ^{Note}	31	W	R	0b	1: Clears DRWE 0: No change
Other		R	R	0b	

Note   These fields can only be reset by hardware reset.

Register: HcRhPortStatus [1:3]   Offset Address: 54h, 58h, 5Ch

These registers are set by the value of Port No field in PCI configuration's EXT1 register as following table. When the invalid register is read, it returns FFFFFFFFh.

Table 4-33. Port No Field vs HcRhPortStatus[1:3]

Port No	OHCI #1			OHCI #2	
	HcRhPortStatus1	HcRhPortStatus2	HcRhPortStatus3	HcRhPortStatus1	HcRhPortStatus2
5	Valid	Valid	Valid	Valid	Valid
4	Valid	Valid	Invalid	Valid	Valid
3	Valid	Valid	Invalid	Valid	Invalid
2	Valid	Invalid	Invalid	Valid	Invalid

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Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HC		
CurrentConnectStatus (CCS)[Note]	0	R	R/W	0b	This bit reflects the current state of the downstream port. 0: no device connected 1: device connected
ClearPortEnable (CPE)[Note]		W	R	0b	The HCD writes a '1' to this bit to clear the PES bit. Writing a '0' has no effect. The CCS is not affected by any write. Note: This bit is always read '1b' when the attached device is non-removable.
PortEnableStatus (PES)[Note]	1	R	R/W	0b	This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PESC to be set. HCD clears it by writing CPE. This bit cannot be set when CCS is cleared. This bit is also set, if not already, at the completion of a port reset when RSC is set or port suspend when SSC is set. 0: port is disabled 1: port is enabled
SetPortEnable (SPE)[Note]		R	W	0b	According to OHCI spec, HCD can set PES by writing a '1'. However, the HCD can not set PES in this core by writing a '1' to comply with USB1.1 spec. Writing a '0' has no effect. If CCS is cleared, this write does not set PES, but instead sets CSC. This informs the driver that it attempted to enable a disconnected port.

Note These fields can only be reset by hardware reset.

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Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HC		
PortSuspendStatus (PSS) [Note]	2	R	R/W	0b	This bit indicates the port is suspended or in the resume sequence. It is set by a SPS write and cleared when PSSC is set at the end of the resume interval. This bit cannot be set if CCS is cleared. This bit is also cleared when PRSC is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0: port is not suspended 1: port is suspended
SetPortSuspend (SPS) [Note]		W	R	0b	The HCD sets the PSS bit by writing a '1' to this bit. Writing a '0' has no effect. If CCS is cleared, this write does not set PSS; instead it sets CSC. This informs the driver that it attempted to suspend a disconnected port.
PortOverCurrentIndicator (POCI) [Note]	3	R	R/W	0b	This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0: no overcurrent condition. 1: overcurrent condition detected.
ClearSuspendStatus (CSS) [Note]		W	R	0b	The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PSS is set.
PortResetStatus (PRS) [Note]	4	R	R/W	0b	When this bit is set by a write to SPR, port reset signaling is asserted. When reset is completed, this bit is cleared when PRSC is set. This bit cannot be set if CCS is cleared. 0: port reset signal is not active 1: port reset signal is active
SetPortReset (SPR) [Note]		W	R	0b	The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CCS is cleared, this write does not set PRS, but instead sets CSC. This informs the driver that it attempted to reset a disconnected port.
Reserved	7 : 5	R	R	0h	Reserved

Note   These fields can only be reset by hardware reset.

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| Field | Bit | Read/Write | | Value | Comment |
		HCD	HC	(Default)	
PortPowerStatus (PPS)^{Note}	8	R	R/W	0b	This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SPP or SGP. HCD clears this bit by writing CPP or CGP. Which power control switches are enabled is determined by PSM and PPCM. In global switching mode (PSM = 0), only SGP/CGP controls this bit. In per-port power switching (PSM = 1), if the PPCM bit for the port is set, only SPP/CPP commands are enabled. If the mask is not set, only SGP/CGP commands are enabled. When port power is disabled, CCS, PES, PSS, and PRS should be reset. 0: port power is off 1: port power is on
SetPortPower (SPP) ^{Note}		W	R	0b	The HCD writes a '1' to set the PPS bit. Writing a '0' has no effect. Note: This bit is always reads '1b' if power switching is not supported.
LowSpeedDeviceAttached (LSDA) ^{Note}	9	R	R/W	0b	This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CCS is set. 0: full speed device attached 1: low speed device attached
ClearPortPower (CPP) ^{Note}		W	R	0b	The HCD clears the PPS bit by writing a '1' to this bit. Writing a '0' has no effect.
Reserved	15 : 10	R	R	0h	Reserved
ConnectStatusChange (CSC) ^{Note}	16	R/W	R/W	0b	This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CCS is cleared when a SPR, SPE, or SPS write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0: no change in CCS 1: change in CCS Note: If the DR bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.

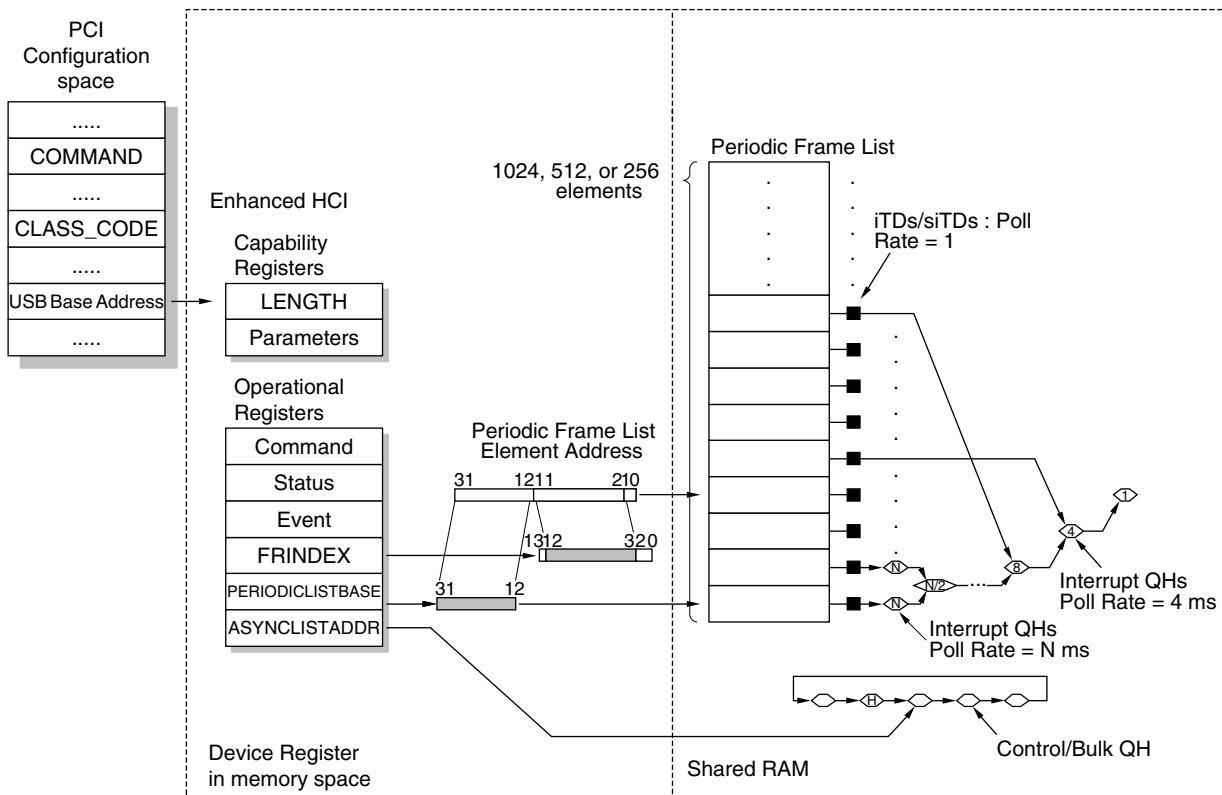**Note** These fields can only be reset by hardware reset.

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Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HC		
PortEnableStatusChange (PESC) Note	17	R/W	R/W	0b	This bit is set when hardware events cause the PES bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: no change in PES 1: change in PES
PortSuspendStatusChange (PSSC) Note	18	R/W	R/W	0b	This bit is set when the full resume sequence has been completed. This sequence includes the 20-ms resume pulse, LS EOP, and 3-ms resynchronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when PRSC is set. 0: resume is not completed 1: resume completed
PortOverCurrentIndicator Change (OCIC) Note	19	R/W	R/W	0b	This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the POCI bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: no change in POCI 1: POCI has changed
PortResetStatusChange (PRSC) Note	20	R/W	R/W	0b	This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: port reset is not completed 1: port reset is completed
Reserved	31 : 21	R	R	0h	Reserved

Note These fields can only be reset by hardware reset.

4.3 EHCI Capability and Operational Registers

The EHCI Host controller includes a set of read only Capability Registers and a set of read/write Operational Registers, which are the starting point for communication with the host CPU. The PCI Configuration Space's Base Address Register in EHCI Host Controller indicates the base address of Capability Registers. The Operational Register base must be calculated by adding the value in the first Capabilities Register (CAPLENGTH) to the EHCI Host Controller register address space. These sets of registers are mapped to a 256 bytes range in the 4-Gbyte main memory spaces. All of the registers should be read and written as Dwords. For a more detailed description, see the **EHCI Specification Rev. 1.0**.

Figure 4-2. Enhanced HCI's PCI Configuration Space

4.3.1 Mapping of capability and operational registers for EHCI host controller

Table 4-34. Capability and Operational Registers for EHCI Host Controller

31	16	15	8	7	0	Offset
HCIVERSION		Reserved		CAPLENGTH		00h
HCSPARAMS						04h
HCCPARAMS						08h
HCSP_PORTROUTE						0Ch
USBCMD						20h
USBSTS						24h
USBINTR						28h
FRINDEX						2Ch
CTRLDSSEGMENT						30h
PERIODICLISTBASE						34h
ASYNCLISTADDR						38h
Reserved						3Ch 5Fh
CONFIGFLAG						60h
PORTSC1						64h
PORTSC2						68h
PORTSC3						6Ch
PORTSC4						70h
PORTSC5						74h
Reserved						78h E8h
NEC private Reg. 1						ECh
NEC private Reg. 2						F0h
I2C_CMD						F4h
I2C_WND0						F8h
I2C_WND1						FCh

Remark   Prohibits accessing NEC private Reg. X which are allocated to offset address ECh-F0h.

4.3.2 Overview of EHCI capability and operational registers

Register: CAPLENGTH   **Offset Address: 00h**

Field	Bit	Read/Write HCD	Value (Default)	Comment
Capability Registers Length	7 : 0	R	20h	Offset address for the beginning of operational registers.

Register: HCIVERSION   **Offset Address: 02h**

Field	Bit	Read/Write HCD	Value (Default)	Comment
Interface Version Number	15 : 0	R	10h	Complies with Enhanced HCI R1.0

Register: HCSPARAMS   **Offset Address: 04h**

Field	Bit	Read/Write HCD	Value (Default)	Comment
Number of Ports (N_PORTS)	3:0	R	0101b	Indicates the number of physical downstream ports on EHCI HC. This bit is reflected by the value of *Port No* field in PCI configuration space's EXT1 reg.
Port Power Control (PPC)	4	R	1b	This bit is reflected by the value of *PPC_setting* bit in PCI configuration space's EXT1 reg. 0: HC does not have the port power control switches. And then, port power is always active. 1: HC has the port power control switches. If port power is always active, this bit should be set to a zero by *PPC_setting* bit and NPS bit in OHCI's HcRhDescriptorA reg. should be set to a one.
Reserved	6 : 5	R	00b	Reserved
Port Routing Rules	7	R	1b	The port routing is explicitly enumerated by the first *N_PORTS* elements of the *HCSP_PORTROUTE* array.

Number of Ports per Companion Controller (N_PCC)	11 : 8	R	0011b	Indicates the number of ports supported companion OHCI host controllers. This bit is reflected by the value of *Port No* field in PCI configuration space's EXT1 reg.
				
				Port No N_PORTS N_PCC
				  5 5 3
				  4 4 2
				  3 3 2
				  2 2 1

Number of Companion Controller (N_CC)	15 : 12	R	0010b	Indicates the number of companion OHCI host controllers associated with EHCI HC.
Port Indicators (P_INDICATOR)	16	R	0b	HC does not support the port indicator control.
Reserved	19 : 17	R	0h	Reserved
Debug Port Number	23 : 20	R	0000b	HC does not support the debug port.
Reserved	31 : 24	R	0h	Reserved

Register: HCCPARAMS   **Offset Address: 08h**

Field	Bit	Read/Write HCD	Value (Default)	Comment
64-bit Addressing Capability	0	R	0b	Data structure using 32-bit address memory pointers.
Programmable Frame List Flag	1	R	1b	HCD can specify and use a smaller frame list and configure HC (EHCI) via the USBCMD register *Frame List Size* field.
Asynchronous Schedule Park Capability	2	R	1b	This bit indicates whether HC supports the park feature for high-speed queue heads in the Asynchronous schedule.
Reserved	3	R	00b	Reserved
Isochronous Scheduling Threshold	7 : 4	R	0000b	HC does not support to cache the isochronous data structure for an entire frame.
EHCI Extended Capabilities Pointer (EECP)	15 : 8	R	E8h	This optional register indicates the existence of a capabilities list and offset in PCI configuration space of the first EHCI extended capability.
Reserved	31 : 16	R	0h	Reserved

Register: HCSP_PORTROUTE   **Offset Address: 0Ch**

Field	Bit	Read/Write HCD	Value (Default)	Comment
Companion Port Route	31 : 0	R	01010h	Port 1, 3, and 5 are routed to OHCI #1. Port 2 and 4 are routed to OHCI #2.

Register: USBCMD   **Offset Address: 20h**

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Field	Bit	Read/Write HCD	Value (Default)	Comment
Run/Stop (RS)	0	R/W	0b	0: Stop (HC completes the current transaction on the USB and then halts.) 1: Run (HC proceeds with execution of the schedule.) HC continues execution as long as this bit is set to a one. The *HCHalted* bit in the USBSTS register indicates when HC has finished the transaction and has entered the stopped state. HCD should not write a one unless HC is in the Halted state.
Host Controller Reset (HCRESET)	1	R/W	0b	When HCD writes a one, HC resets its internal pipelines, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to companion (OHCI) host controller(s). When the reset process is complete, HC sets to a zero. HCD cannot terminate the reset process early by writing a zero. HCD should not set this bit to a one when the *HCHalted* bit is a zero.
Frame List Size	3 : 2	R/W	00b	Specifies the size of the frame list. The FRINDEX register should be used for the Frame List Current index. 00b: 1024 elements (4096 bytes) 01b: 512 elements (2048 bytes) 10b: 256 elements (1024 bytes) 　　- for resource-constrained environments 11b: Reserved
Periodic Schedule Enable	4	R/W	0b	Controls whether HC skips processing the Periodic Schedule. 0: Do not process the Periodic Schedule. 1: Use the PERIODICLISTBASE register to access the Periodic Schedule
Asynchronous Schedule Enable	5	R/W	0b	Controls whether HC skips processing the Asynchronous Schedule. 0: Do not process the Asynchronous Schedule. 1: Use the ASYNCLISTADDR register to access the Asynchronous Schedule

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Field	Bit	Read/Write HCD	Value (Default)	Comment
Interrupt on Async Advance Doorbell	6	R/W	0b	HCD uses this bit as a doorbell to tell HC to issue an interrupt at the next interrupt threshold when it advances next queue head. HCD must write a one to *ring* the doorbell.
				When HC has evicted all appropriate cached schedule state, it sets the *interrupt on Async Advance* bit in the USBSTS register.
				HC sets to a zero after it has set the *Interrupt on Async Advance* bit to a one.
Light Host Controller Reset	7	R	0b	HC does not support the light HC Reset
Asynchronous Schedule Park Mode Count	9 : 8	RW	11b	This field counts the number of successive transactions HC can execute from one queue head.
Reserved	10	R	0h	Reserved
Asynchronous Schedule Park Mode Enable	11	RW	1b	This bit indicate Park mode enable/disable. 0 : disable 1 : enable
Reserved	15 : 12	R	0h	Reserved
Interrupt Threshold Control	23 : 16	R/W	08h	Indicates the maximum rate at which HC will issue interrupts.

Interrupt Threshold Control comment table:

Value	Maximum Interrupt Interval
00h:	Reserved
01h:	1 micro-frame
02h:	2 micro-frames
04h:	4 micro-frames
08h:	8 micro-frames (1 ms)
10h:	16 micro-frames (2 ms)
20h:	32 micro-frames (4 ms)
40h:	64 micro-frames (8 ms)

Any other value yields undefined result.

Field	Bit	Read/Write HCD	Value (Default)	Comment
Reserved	31 : 24	R	0h	Reserved

Register: USBSTS **Offset Address: 24h**

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Field	Bit	Read/Write HCD	Value (Default)	Comment
USB Interrupt (USBINT)	0	R/W	0b	HC sets it to a one when the cause of an interrupt is a completion of a USB transaction. HC also sets to a one when a short packet is detected (actual number of bytes received was less than the expected number of bytes). HCD writes a one to clear this bit. Writing a zero has no effect.
USB Error Interrupt (USBERRINT)	1	R/W	0b	HC sets it to a one when completion of a USB transaction results in an error condition (e.g. error counter underflow). HCD writes a one to clear this bit. Writing a zero has no effect.
Port Change Detect	2	R/W	0b	HC sets it to a one when any port for which the *Port Owner* bit in the PORTSC[n] register is set to zero is satisfied one of following conditions. A change bit of port transitions from a zero to a one. A PORTSC[n] register *Force Port Resume* bit of port transitions from a zero to a one as a result of a J-K transition detected on a suspended port. It is acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC[n] register change bits (including *Force Port Resume, Over-current Change, Port Enable/Disable Change,* and *Connect Status Change*) HCD writes a one to clear this bit. Writing a zero has no effect.
Frame List Rollover	3	R/W	0b	HC sets it to a one when the *Frame Index* field in the FRINDEX register rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. HCD writes a one to clear this bit. Writing a zero has no effect.
Host System Error	4	R/W	0b	HC sets it to a one when a serious error occurs during a host system access involving the HC module. In a PCI system, HC sets this bit to a one by PCI Parity error, etc. When this error occurs, the HC clears the *RS* bit in the USBCMD register to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system. HCD writes a one to clear this bit. Writing a zero has no effect.

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Field	Bit	Read/Write	Value	Comment
		HCD	(Default)	
Interrupt on Async Advance	5	R/W	0b	When HC fetch QH, It will check whether *Interrupt on Async Advance Doorbell* bit in the USBCMD register is a one or not. If *Interrupt on Async Advance Doorbell* bit is a one, HC will issue this interrupt at the next interrupt threshold when HC advances next queue head. HCD writes a one to clear this bit. Writing a zero has no effect.
Reserved	11 : 6	R	0h	Reserved
HCHalted	12	R	1b	This bit is a zero whenever the *RS* bit in the USBCMD register is a one. HC sets to a one after it has stopped executing as a result of the *RS* bit being set to a zero, either by HCD or by HC hardware (e.g. internal error)
Reclamation	13	R	0b	This is used to detect an empty asynchronous schedule. When HC fetches Queue Head with H = 1 or after reset, HC set it to a zero. When HC executes async transaction or detects start event, HC set it to a one. If HC fetches Queue Head with H = 1 and this bit is a zero, HC transtions to Async Sched sleeping mode.
Periodic Schedule Status	14	R	0b	Reports the current real status of the Periodic Schedule. 0: The Periodic Schedule is disabled. 1: The Periodic Schedule is enabled. When this bit and the *Periodic Schedule Enable* bit in the USBCMD register are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
Asynchronous Schedule Status	15	R	0b	Reports the current real status of the Asynchronous Schedule. 0: The Asynchronous Schedule is disabled. 1: The Asynchronous Schedule is enabled. When this bit and the *Asynchronous Schedule Enable* bit in the USBCMD register are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
Reserved	31 : 16	R	0h	Reserved

Register: USBINTR   **Offset Address: 28h**

Field	Bit	Read/Write HCD	Value (Default)	Comment
USB Interrupt Enable	0	R/W	0b	0: Ignore 1: The *USBINT* bit in the USBSTS register is a one, HC will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by HCD clearing the *USBINT* bit.
USB Error Interrupt Enable	1	R/W	0h	0: Ignore 1: The *USBERRINT* bit in the USBSTS register is a one, HC will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by HCD clearing the *USBERRINT* bit.
Port Change Interrupt Enable	2	R/W	0b	0: Ignore 1: The *Port Change Detect* bit in the USBSTS register is a one, HC will issue an interrupt immediately. The interrupt is acknowledged by HCD clearing the *Port Change Defect* bit.
Frame List Rollover Enable	3	R/W	0b	0: Ignore 1: The *Frame List Rollover* bit in the USBSTS register is a one, HC will issue an interrupt immediately. The interrupt is acknowledged by HCD clearing the *Frame List Rollover* bit.
Host System Error Enable	4	R/W	0b	0: Ignore 1: The *Host System Error* bit in the USBSTS register is a one, HC will issue an interrupt immediately. The interrupt is acknowledged by HCD clearing the *Host System Error* bit.
Interrupt on Async Advance Enable	5	R/W	0b	0: Ignore 1: The *Interrupt on Async Advance* bit in the USBSTS register is a one, HC will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by HCD clearing the *Interrupt on Async Advance* bit.
Reserved	31 : 6	R	0h	Reserved

Register: FRINDEX   **Offset Address: 2Ch**

Field	Bit	Read/Write	Value	Comment
		HCD	(Default)	

Frame Index	13 : 0	R/W	00h	The value in this register increments at the end of each micro-frame. Bits [N:3] are used for the Frame List Current index. This means that each location of the frame list is accessed 8 times before moving to the next index.
				
				Frame List Size Number
				Elements N
				00b (1024)
				          12
				01b (512)
				          11
				10b (256)
				          10
				11b Reserved
				
				This register cannot be written unless HC is in the Halted state as indicated by the *HCHalted* bit.
				
				Writes to this register also effect the SOF value. The SOF frame number value for the bus SOF token is derived from this register.

Reserved	31 : 14	R	0h	Reserved

Register: CTRLDSSEGMENT   **Offset Address: 30h**

Field	Bit	Read/Write	Value	Comment
		HCD	(Default)	
CTRLDSSEGMENT	31 : 0	R	00h	*64-bit Addressing Capability* field in HCCPARAMS register is a zero, so this register is not used. HCD cannot write to it.

Register: PERIODICLISTBASE   **Offset Address: 34h**

Field	Bit	Read/Write	Value	Comment
		HCD	(Default)	
Reserved	11 : 0	R	0h	Reserved (The memory structure is assumed to be 4-Kbyte aligned.) During runtime, the values of these bits are undefined.
BaseAddress(Low)	31 : 12	R/W	XXh	Contains the beginning address of the Periodic Frame List in the system memory. HCD loads this register prior to starting the schedule execution by HC. The contents of this register are combined with the *Frame Index* field in the FRINDEX register to enable HC to step through the Periodic Frame List in sequence.

Register: ASYNCLISTADDR   **Offset Address: 38h**

Field	Bit	Read/Write	Value	Comment
		HCD	(Default)	
Reserved	4 : 0	R	0h	Reserved (The memory structure is assumed to be 32-byte aligned.) This value has no effect on operation.
Link Pointer Low(LPL)	31 : 5	R/W	XXh	Contains the address of the next asynchronous queue head to be executed.

Register: CONFIGFLAG   **Offset Address: 60h**

Field	Bit	Read/Write	Value	Comment
		HCD	(Default)	
Configure Flag (CF)	0	R/W	0b	HCD sets this bit as the last action in its process of configuring the HC. This bit controls the default port-routing control logic. 0: Port routing control logic default-routes each port to an implementation dependent companion (OHCI) host controller. 1: Port routing control logic default-routes all ports to EHCI HC.
Reserved	31 : 1	R	0h	Reserved

Remark It is only reset by hardware when the auxiliary power is initially applied or in response to a host controller reset.

Register: PORTSC [1:5]   **Offset Address: 64h, 68h, 6Ch, 70h, 74h**

These registers are set by the value of Port No field in PCI configuration's EXT1 register as following table. When the invalid register is read, it returns FFFFFFFFh.

Port No	EHCI				
	PORTSC1	PORTSC2	PORTSC3	PORTSC4	PORTSC5
5	Valid	Valid	Valid	Valid	Valid
4	Valid	Valid	Valid	Valid	Invalid
3	Valid	Valid	Valid	Invalid	Invalid
2	Valid	Valid	Invalid	Invalid	Invalid

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Field	Bit	Read/Write HCD	Value (Default)	Comment
Current Connect Status	0	R	0b	This value reflects the current state of the port. 1: Device is present on port. 0: No device is present. This field is zero if *PP* bit (bit 12) is zero.
Connect Status Change	1	R/W	0b	Indicates a change has occurred in the port's Current Connect Status bit. HC sets this bit for all changes to the port device connect status, even if HCD has not cleared an existing connect status change. 1: Change in Current Connect Status 0: No change HCD writes a one to clear this bit. Writing a zero has no effect. This field is zero if *PP* bit (bit 12) is zero.
Port Enabled/Disabled	2	R/W	0b	Ports can only be enabled by HC as a part of the reset and enable. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by HCD. Note that the bit status does not change until the port state actually changes. When the port is disabled (0b) downstream propagation of data is blocked on this port, except for reset. 1: Enable 0: Disable This field is zero if *PP* bit (bit 12) is zero.
Port Enable/Disable Change	3	R/W	0b	1: Port Enabled/Disabled status has changed. 0: No change. For the root hub, this bit gets set to a one only when a port is disabled due to disconnect on the *port or* due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification). HCD writes a one to clear this bit. Writing a zero has no effect. This field is zero if *PP* bit (bit 12) is zero.

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Field	Bit	Read/Write HCD	Value (Default)	Comment
Over-current Active	4	R	0b	1: The port currently has an over-current. 0: The port does not have an over-current. This will automatically transition from a one to a zero when the over current is removed.
Over-current Change	5	R/W	0b	1: Over-current Active status has changed. 0: No change. HCD writes a one to clear this bit. Writing a zero has no effect.
Force Port Resume	6	R/W	0b	1: Resume detected/driven on port. 0: No resume (K-state) detected/driven on port. HC sets it to a one and the *Port Change Detect* bit in the USBSTS register is also set to a one if a J-to-K transition is detected while the port is in the suspend state. HCD sets it to a one to drive resume signaling. At that time, HC must not set the *Port Change Detect* bit. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. HCD must set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. This field is zero if *PP* bit (bit 12) is zero.
Suspend	7	R/W	0b	1: Port is in suspend state. 0: Port is not in suspend state. *Port Enabled/Disabled* bit (bit 2) and this bit define the port states as follows. *Port Enabled/Disabled* *Suspend* Port State 0 X Disable 1 0 Enable 1 1 Suspend When in suspend state downstream propagation of data is blocked on this port, except for port reset. The blocking and bit status change occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a one. HC will unconditionally set to a zero when : · HCD sets the *Force Port Resume* bit (bit 6) to a zero. · HCD sets the *Port Reset* bit (bit 8) to a one. This field is zero if *PP* bit (bit 12) is zero.

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Field	Bit	Read/Write HCD	Value (Default)	Comment
Port Reset	8	R/W	0b	1: Port is in Reset. 0: Port is not in Reset. When HCD writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2 0 is started. HCD writes a zero to this bit to terminate the bus reset sequence. HCD must keep this bit a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2 0, completes. HCD should not attempt to reset a port if the *HCHalted* bit in the USBSTS register is a one. This field is zero if *PP* bit (bit 12) is zero.
Reserved	9	R	0b	Reserved
Line Status	11 : 10	R	00b	These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits[11:10] USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset. This value of this field is undefined if *Port Power* is zero.
Port Power (PP)	12	R/W	0b	The function of this bit depends on the value of the *Port Power Control (PPC)* field in the HCSPARAMS register. The behavior is as follows: PPC PP Operation 0b 1b HC does not have port power control switches. Each port is hard-wired to power. 1b 1b/0b HC has port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (i.e. *PP* equals a 0), the port is nonfunctional and will not report attaches, detaches, etc. When an over current condition is detected on a powered port and *PPC* is a one, the *PP* bit in each affected port may be transitioned by HC from a one to a zero (removing power from the port).
Port Owner	13	R/W	1b	This bit unconditionally goes to a zero when the *Configured Flag* bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to a one whenever the *Configured Flag* bit is zero. HCD uses this field to release ownership of the port to a selected HC. HCD writes a one to this bit when the attached device is not a high-speed device.

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Field	Bit	Read/Write HCD	Value (Default)	Comment
Port Indicator Control	15 : 14	R	00b	The *P_INDICATOR* bit in the HCSPARAMS register is a zero. So, writing to this bit has no effect.
Port Test Control	19 : 16	R/W	0000b	When this field is zero, the port is NOT operating in a test mode. The encoding of the test mode bits are (0110b -1111b are reserved) Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE 0010b Test K_STATE 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2 0, Chapter 7 for details on each test mode.
Wake on Connect Enable (WKCNNT_E)	20	R/W	0b	Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. This bit does not affect operation when HC is running. This field is zero if *PP* bit (bit 12) is zero.
Wake on Disconnect Enable (WKDSCNNT_E)	21	R/W	0b	Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This bit does not affect operation when HC is running. This field is zero if *PP* bit (bit 12) is zero.
Wake on Over-current Enable (WKOC_E)	22	R/W	0b	Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. This bit does not affect operation when HC is running. This field is zero if *PP* bit (bit 12) is zero.
Reserved	31 : 23	R	0h	Reserved

Remarks 1. HCD uses this information as an input parameter to determine how many ports need to be serviced.

2. It is only reset by hardware when the auxiliary power is initially applied or in response to a host controller reset. The initial conditions of a port are a
• No device connected,
• Port disabled

Register: I2C_CMD   **Offset Address: F4h**

Register: I2C_WND0   **Offset Address: F8h**

Register: I2C_WND1   **Offset Address: FCh**

 Refer **CHAPTER 8 HOW TO WRITE EXTERNAL SERIAL ROM** for detail information about these three registers.

4.4 Legacy Function Registers

The μPD720101 includes the Legacy Function Registers, which emulate legacy keyboard and mouse. When "LEGC" pin is clamped to "high", this function can be used. System software can access to 100h-10Ch memory address spaces to realize emulation for legacy keyboard and mouse. And I/O access for 60h/64h will be controlled by Legc_mode bit which is allocated in EXT1 register of configuration space. When Legc_mode is set to "low", HC will intercept 60h/64h I/O access even if PCI Configuration Space's Base Address (I/O Address) Register in OHCI Host Controller #1 is not set to "60h" by BIOS. If Legc_mode is set to "high" and Legacy Function is enabled, PCI I/O Address Register in OHCI Host Controller #1 to "60h" should be set by BIOS. When PCI I/O address register is set to "60h", HC intercepts 60h/64h I/O access. This set of registers is mapped to both memory and I/O space, where it is used by the HCD (Host Controller Driver). For a more detailed description, see the **OpenHCI Legacy Support Interface Specification Release Version 1.01**.

4.4.1 Overview of legacy function registers

Table 4-35. Mapping of Legacy Function Registers

Register	Memory Address Offset	I/O Address	Read/Write HCD	Comment
HceControl	100h		R/W	This register is used to enable and control the emulation hardware and report various information.
HceStatus	10Ch		R/W	This is the legacy status register for emulation. Input from port 64h indicates the current value of HceStatus without causing other operations.
		64h (IN)	R	
HceInput	104h		R/W	This is the legacy input buffer register for emulation. Output to port 60h sets "1" to InputFull and "0" to CmdData in the HceStatus register.Output to port 64h sets "1" to InputFull and CmdData in the HceStatus register.
		60h (OUT)	W	
		64h (OUT)	W	
HceOutput	108h		R/W	This is the legacy output buffer register for emulation in which software writes to a keyboard or mouse device. Input from port 60h sets "0" to OutputFull in the HceStatus register.
		60h (IN)	R	

Remark When emulation is enabled (valid), the HceStatus, HceInput, and HceOutput registers can be accessed by I/O addresses 60h and 64h.

Register: HceInput

Field	bit	Read/Write HCD	Value (Default)	Comment
InputData	7 : 0	R/W	Xh	This register retains the data that is written to I/O ports 60h and 64h when emulation is enabled.
Reserved	31 : 8	R	0h	Reserved

Register: HceOutput

Field	bit	Read/Write HCD	Value (Default)	Comment
OutputData	7 : 0	R/W	Xh	This register retains the data that is returned when the application software reads from port 60h and emulation is enabled.
Reserved	31 : 8	R	0h	Reserved

Register: HceStatus

Field	bit	Read/Write HCD	Value (Default)	Comment
OutputFull	0	R/W	0b	When I/O port 60h is read, "0" is set by the HC. When IRQEn is set and AuxOutputFull is set to "0", IRQ1 occurs as long as this bit is set to "1". When IRQEn is set and AuxOutputFull is set to "1", IRQ12 occurs as long as this bit is set to "1". When this bit is "0" and HceControl's CharacterPending is set to "1", the emulation interrupt condition exists.
InputFull	1	R/W	0b	This bit is set to "1" during an I/O write operation to address 60h and 64h, except for the case of the GateA20 sequence. When this bit is set to "1", the emulation interrupt condition exists as long as emulation is enabled.
Flag	2	R/W	0b	This bit is used as a system flag by software to indicate warm/cold boot status.
CmdData	3	R/W	0b	This bit is set to "0" by the HC when writing to port 60h and This bit is set to "1" by the HC when writing to port 64h.
Inhibit Switch	4	R/W	0b	This bit indicates the status of the keyboard inhibit switch. It is set when the keyboard is not inhibited.
AuxOutputFull	5	R/W	0b	IRQ12 is asserted whenever this bit is set to "1" and OutputFull is set to "1" and IRQEn bit is set.
Timeout	6	R/W	0b	This bit is used to indicate a timeout condition.
Parity	7	R/W	0b	This bit indicates a keyboard/mouse data parity error.
Reserved	31 : 9	R	0h	Reserved

Register: HceControl

Field	bit	Read/Write HCD	Value (Default)	Comment
EmulationEnable	0	R/W	0b	When this bit is set to "1", the HC is able to perform legacy emulation. The HC decodes access to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. The HC may also generate an emulation interrupt when necessary to call up the emulation software.
EmulationInterrupt	1	R	0b	This bit is used to static decode emulation interrupt conditions. This bit becomes "1" when emulation interrupt status is ON.
CharacterPending	2	R/W	0b	When this bit is set, an emulation interrupt occurs if the HceStatus register's OutputFull bit is set to "0".
IRQEn	3	R/W	0b	When this bit is set, the HC generates IRQ1 or IRQ12 if the HceStatus register's OutputFull bit is set to "1". Specifically, IRQ1 occurs when the HceStatus register's AuxOutputFull bit is set to "0" and IRQ12 occurs when it is set to "1".
ExternalIRQEn	4	R/W	0b	When this bit is set to "1", an emulation interrupt is triggered by IRQ1 and IRQ12 from the keyboard controller. The function that controls this bit does not depend on the setting of the EmulationEnable bit in this register.
GateA20Sequence	5	R/W	0b	When D1h is written to I/O port 64h, this bit is set by the HC. When a value other than D1h is written to I/O port 64h, this bit is cleared.
IRQ1Active	6	R/W	0b	This bit indicates a positive transition IRQ1 from the keyboard controller has occurred. Software writes "1" to clear this bit. Writing a zero has no effect.
IRQ12Active	7	R/W	0b	This bit indicates a positive transition on IRQ12 from the keyboard controller has occurred. Software writes "1" to clear this bit. Writing a zero has no effect.
A20State	8	R/W	0b	This bit indicates the current status of the keyboard controller's GateA20. When GateA20Sequence is active, this bit is used for comparison with the value that was written to 60h.
Reserved	31 : 9	R	0h	Reserved

CHAPTER 5 OHCI HOST CONTROLLER

OpenHCI is the specifications that apply to the relation between the host controller and the HCD software. This chapter provides an OHCI host controller's communication flow and the data structure that is used. For details, see the **Open Host Controller Interface Specification Release 1.0a.**

5.1 Communication Between OHCI Host Controller and HCD

The OHCI host controller (HC) and the host controller driver (HCD) communicate via the following two paths.

- Operational registers
- Host Controller Communications Area (HCCA)

In communication that uses the operational registers which are built into the OHCI HC, the OHCI HC is the PCI target device. For details of operational registers, see section 4.2. They also include pointers that indicate the position of the HCCA (Host Controller Communications Area) within system memory. The OHCI HC becomes the PCI bus master for communications that are executed via the HCCA. The HCCA is a 256-byte system memory area that contains head pointers to the interrupt ED list, head pointers to the Done Queue, and frame-related status information. The software uses this system memory to directly control the HC's functions without reading from the HC, as long as operation conditions are normal (i.e., there are no errors). These two paths are used for handling HC control tasks and USB data transfer results.

The HCD executes communication between the HC and USB devices, based on the enqueued ED (Endpoint Descriptor) and TD (Transfer Descriptor). An ED contains information (maximum packet size, endpoint address, endpoint speed and data flow direction) that the HC requires to communicate with the endpoint, and the ED can also be used as the TD queue's anchor. The HCD generates EDs and assigns them to the various endpoints, when are then listed and linked.

A TD contains information (data toggle information, buffer positions in system memory, and complete status code) that is required for the data packet to be sent. Each TD also contains information (data buffer size ranging from 0 to 8192 bytes, with a maximum of 1023-byte transfer per data packet) that is related to at least one data packet. Enqueued TDs are serviced in FIFO order. The TD queue is linked with a certain endpoint's ED and the TDs are linked with the TD queue. The HCD generates data from this structure and passes the data to the HC for processing.

5.2 Endpoint Descriptor

An ED is always allocated in 16-byte units to system memory. When the ED list is referenced, if it contains a TD that is linked to an ED, the HC executes the transfer specified by that TD. If the HCD must change the head pointer (HeadP) value, list servicing for all EDs that have the same transfer type as the ED to be deleted must be rendered invalid so as to prevent the HC from accessing the EDs. Therefore, the HCD sets a Skip bit.

5.2.1 Endpoint descriptor format

Table 5-1. Endpoint Descriptor Format

	31 27	26	16 15	14	13	12 11	10 07	06 04	03 02 01 00
Dword0	-	MPS	F	K	S	D	EN		FA
Dword1	TD Queue Tail Pointer (TailP)								-
Dword2	TD Queue Head Pointer (HeadP)							0	C H
Dword3	Next Endpoint Descriptor (NextED)								-

5.2.2 Endpoint descriptor field definitions

Table 5-2. Description of Endpoint Descriptors

(1/2)

Name	HC Access	Description
FA	R	Function Address USB address of function that includes the endpoint that is controlled by this ED
EN	R	Endpoint Number Endpoint address in function
D	R	Direction Indicates the data flow direction (IN or OUT). If neither IN nor OUT are specified, the transfer direction is defined by the TD's PID (Packet ID) field. <table><tr><th>Code</th><th>Direction</th></tr><tr><td>00b</td><td>Get direction From TD</td></tr><tr><td>01b</td><td>OUT</td></tr><tr><td>10b</td><td>IN</td></tr><tr><td>11b</td><td>Get direction From TD</td></tr></table>
S	R	Speed This indicates the endpoint's speed. • full-speed (S = 0) • low-speed (S = 1)
K	R	Skip When this bit is set, the HC proceeds to the next ED without accessing the TD queue or issuing a USB token to the endpoint.
F	R	Format This indicates the format of a TD that is linked to this ED. For control, bulk, or interrupt endpoints, if F = 0, then the General TD format is used. For isochronous endpoints, if F = 1, the Isochronous TD format is used.

Name	HC Access	Description
MPS	R	Maximum Packet Size This field indicates the maximum number of bytes (1023 bytes) per data packet that can be received from the endpoint or sent to an endpoint. When a write operation (OUT or SETUP) is executed from the HC to the endpoint, the size of the data packet to be sent always becomes either the Maximum Packet Size or the size of the data in the buffer, whichever is smaller. When a read operation (IN) is executed from the endpoint to the HC, the data packet size is determined according to the endpoint.
TailP	R	TD Queue Tail Pointer When TailP and HeadP have the same value, the list does not contain any TDs that can be serviced by the HC. When the TailP and HeadP values are different, the list contains TDs.
H	R/W	Halted This bit is set by the HC to indicate when servicing of the endpoint TD queue has been suspended due to a normal TD servicing error.
C	R/W	toggle Carry This bit is the data toggle carry bit. Whenever a TD is retired, the last data toggle value (LSb in the data Toggle field) that was used by the retired TD is written. This field cannot be used by isochronous endpoints.
HeadP	R/W	TD Queue Head Pointer This indicates the next TD to be serviced at this endpoint.
NextED	R	Next ED When its value is other than zero, this bit indicates the next ED.

5.3 Transfer Descriptors

TDs (Transfer Descriptors) are used by the HC to indicate the buffer for the data that is sent to or from an endpoint. TDs are divided into two types: General TDs and Isochronous TDs. General TDs are used by interrupt, control, and bulk endpoints while Isochronous TDs are used for handling isochronous transfers.

For both General and Isochronous TDs, buffers ranging from 0 bytes to 8,192 bytes can be indicated. Also, the data buffer described by one TD can be divided into two pages. This enables the elimination of various problems, such as problems related to forced physical connection of buffers or transfer of surplus data.

When the HCD appends a TD, the TD indicated by TailP is linked to the new TD, and TailP is then changed to indicate the appended TD. Therefore, the appended TD is always added to the end of the TD queue. The HC services the TD asynchronously in relation to servicing performed by the host processor. Consequently, when it is necessary to switch from the TD queue to something else, the HC's endpoint TD queue servicing must be suspended to avoid problems from occurring due to this switch. Suspension of TD servicing is achieved when the HCD sets the Skip bit in the ED to be deleted.

5.3.1 General transfer descriptor format

General TDs are used for control, bulk, or interrupt transfers, and they must always be allocated in 16-byte units to system memory.

Table 5-3. General TD Format

	31 28	27 26	25 24	23 21	20 19	18	17 04	03 00
Dword0	CC	EC	T	DI	DP	R	-	
Dword1	Current Buffer Pointer (CBP)							
Dword2	Next TD (Next TD)							0
Dword3	Buffer End (BE)							

5.3.2 General transfer descriptor field definitions

The General TD's Current Buffer Pointer indicates the data buffer address used for a data packet transfer to or from an endpoint. If the transfer is completed without the occurrence of any kind of error, the HC advances the Current Buffer Pointer by exactly the number of transferred bytes. If the buffer address indicated by the Current Buffer Pointer exceeds the 4-K boundary during a data packet transfer, the high-order 20 bits of the Buffer End field is copied to the working value from the Current Buffer Pointer. The next buffer address becomes byte 0 in the same 4-K page space that is used when the final byte is retained.

Table 5-4. Description of General TD

Name	HC Access	Description
R	R	buffer Rounding When this bit's value is "0", the data buffer defined by the last data packet sent from the endpoint specified by the TD must be a completely full buffer. When its value is "1", the data buffer defined by the last data packet is not full, even if there are no errors.
DP	R	Direction/PID This indicates the data flow direction and PID used by a token. This field only has significance in relation to the HC when 00b or 11b is set to indicate that the ED's D field has delayed the PID judgment until the TD. | Code	PID Type	Data Direction
------	----------	----------------
00b	SETUP	to endpoint
01b	OUT	to endpoint
10b	IN	From endpoint
11b	Reserved		
DI	R	Delay Interrupt This indicates the time until a interrupt occurs as notification of completed TD servicing. When the TD has been completed, the HC delays the interrupt event until the frame indicated by this bit. When this bit's value is 111b, interrupts related to completion of this TD do not occur.
T	R/W	Data Toggle This field is used to generate a comparison or occurrence of data PID values (DATA0 or DATA1). This field is updated after each successful transfer of a data packet. When the data Toggle field's Msb is "0", the data Toggle field's Lsb, which was acquired from the ED's toggle Carry bit, is ignored. When data Toggle field's Msb is "1", the data Toggle field's LSb indicates the data toggle.
EC	R/W	Error Count This field is incremented after each transmission error. If an error occurs after the Error Count has reached "2", the type of error is written to the Condition Code field and is transferred to the done queue. If servicing ends without any errors, the Error Count is reset to "0".
CC	R/W	Condition Code This field is updated each time processing is executed, regardless of whether or not the processing was successful. If it was successful, this field is set as NoError. If unsuccessful, it is set according to the type of error.
CBP	R/W	Current Buffer Pointer This includes the next physical address in memory that will be accessed by a transfer from or to an endpoint. A "0" value indicates either that the data packet has zero length or that all bytes have been transferred.
NextTD	R/W	Next TD This specifies the next TD in the TD list linked to the endpoint.
BE	R	Buffer End This indicates the physical address of the last byte in the TD's buffer.

5.3.3 Isochronous transfer descriptor format

Isochronous TDs are used only by isochronous endpoints. All TDs linked to the ED must use this format when F = 1. This TD is allocated to system memory in 32-byte units.

Table 5-5. Isochronous TD Format

	31	28	27	26	24	23	21	20	16	15	12	11	05	04	00
Dword0	CC		-	FC		DI		-				SF			
Dword1	Buffer Page 0 (BP0)									-					
Dword2	NextTD											0			
Dword3	Buffer End (BE)														
Dword4	Offset1/PSW1							Offset2/PSW0							
Dword5	Offset3/PSW3							Offset4/PSW2							
Dword6	Offset5/PSW5							Offset6/PSW4							
Dword7	Offset7/PSW7							Offset8/PSW6							

5.3.4 Isochronous transfer descriptor field definitions

Isochronous TDs have a (Frame Count + 1) frame buffer with a continuous range from 1 to 8. The first data packet is sent when the low-order 16 bits of HcFmNumber matches the Isochronous TD's Starting Frame value. If the buffer address exceeds the 4-K boundary during a data packet transfer, the high-order 20 bits of the Buffer End field is used as the physical address of the next page. Consequently, the next buffer address becomes byte 0 in the same 4-K page space that is used when the final byte is retained.

Table 5-6. Description of Isochronous TD

Name	HC Access	Description
SF	R	Starting Frame This includes the low-order 16 bits of the number of frames sent by the Isochronous TD's first data packet.
DI	R	Delay Interrupt This indicates the time until a interrupt occurs following completion of Isochronous TD servicing.
FC	R	Frame Count This is the number of data packets indicated by the Isochronous TD. When Frame Count = 0, one data packet is included and when Frame Count = 7, eight data packets are included.
CC	R/W	Condition Code This field includes a completion code when an Isochronous TD has been transferred to the Done Queue.
BP0	R	Buffer Page 0 This is the physical page number of the first byte in the data buffer used by the Isochronous TD.
NextTD	R/W	Next TD This indicates the next Isochronous TD in the Isochronous TD queue linked to an ED.
BE	R	Buffer End This includes the physical address of the buffer's last byte.
OffsetN	R	Offset This is used to determine the size and start address of an isochronous data packet.
PSWN	W	Packet Status Word This includes the size of the completion code and the received isochronous data packet.

5.3.5 Packet status word format

Table 5-7. Packet Status Word Format

15 12	11	10 00
CC	0	SIZE

5.3.6 Packet status word field definitions

Table 5-8. Description of Packet Status Word

Name	HC Access	Description
SIZE	R/W	Size of Packet For IN transfers, this field is written the number of bytes which are received from the endpoint. For OUT transfer, this field is written to 0.
CC	R/W	Condition Code This field indicates both completion code and the format of the word. When the Condition Code indicates NOTACCESSED, the data is in Offset format. Otherwise, the SIZE field contains a value that is appropriate to the direction of data flow and the completion status.

5.3.7 Completion code definitions

Table 5-9. Description of Completion Code

Code	Meaning	Description
0000	NOERROR	General TD or isochronous data packet processing completed with no detected errors
0001	CRC	Last data packet from endpoint contained a CRC error
0010	BITSTUFFING	Last data packet from endpoint contained a bit stuffing violation
0011	DATATOGGLEMISMATCH	Last data packet from endpoint had data toggle PID that did not match the expected value.
0100	STALL	TD was moved to the Done Queue.
0101	DEVICENOTRESPONDING	Device did not respond to token (IN) or did not send any handshake (OUT).
0110	PIDCHECKFAILURE	PID from endpoint is failed.
0111	UNEXPECTEDPID	Received PID is undefined or invalid.
1000	DATAOVERRUN	The amount of data returned by the endpoint exceeded either the size of the maximum data packet allowed from the endpoint or the remaining buffer size.
1001	DATAUNDERRUN	The endpoint returned less than Maximum Packet Size and the amount was not sufficient to fill the specified buffer.
1010	Reserved	
1011	Reserved	
1100	BUFFEROVERRUN	During an IN, HC received data from endpoint faster than it could be written to system memory.
1101	BUFFERUNDERRUN	During an OUT, HC could not retrieve data from system memory fast enough to keep up with data USB data rate.
111x	NOTACCESSED	This code is set by software before the TD is placed on a list to be processed by the HC.

5.4 Host Controller Communications Area

The HCCA (Host Controller Communications Area) is a 256-byte area in system memory that is used by the system software for sending and receiving control/status information to and from the HC. The system software always writes the address of the area to the HC's HcHCCA field.

5.4.1 Host controller communications area format

Table 5-10. Description of Host Controller Communications Area

Offset	Size (bytes)	Name	R/W	Description
0	128	HccaInterruptTable	R	This 32-Dword entry table is a pointer to ED interrupt lists.
0×80	2	HccaFrameNumber	W	This includes the current frame number. This value is updated by the HC before periodic list servicing of the frame begins.
0×82	2	HccaPad1	W	When the HC updates the HccaFrameNumber value, the HC sets "0" to this word.
0×84	4	HccaDoneHead	W	When the HC reaches the end of a frame and a decremented value of "0" is shown as the Delay Interrupt value, the HC writes the current HcDoneHead value to this field. At this point, interrupts occur as valid interrupts. The HC does not write again until the software clears the WD bit in the HcInterruptStatus register. If this field has a value of "0", interrupts can occur for reasons other than updating of HccaDoneHead, and the HcInterruptStatus register must be accessed to determine the cause of the interrupt. If this field's value is not "0", the interrupt is due to updating of the Done Queue. If this field's LSb is not "0", another interrupt event has occurred. The HcInterruptStatus field must be checked to determine the cause of that interrupt.
0×88	116	Reserved	R/W	This field is reserved for use by the HC.

5.4.2 Host controller communications area description

HccaInterruptTable is a 32-Dword entry table which functions as a pointer to the ED list's various interrupt lists. The more of these lists that an ED is linked to, the higher the execution rate. The execution rate is 32 ms for an ED that is in only one list, but it is 6 ms for an ED that is in two lists. An ED that is linked to all 32 lists is executed at a rate of once per frame. The last entry in each of the 32 interrupt lists must specify an isochronous list.

After an SOF (Start Of Frame) token is sent, the HC overwrites HccaFrameNumber using the FrameNumber value from HcFmNumber before it starting reading the ED to be serviced in a new frame.

CHAPTER 6 EHCI HOST CONTROLLER

Enhanced HCI is the specifications that apply to the relation between the host controller and the HCD software. This chapter provides the data structure that is used. For details, see the **Enhanced Host Controller Interface Specification Revision 1.0.**

6.1 Control EHCI Host Controller by HCD

The HCD executes communication between the HC and USB devices, based on the enqueued iTD (Isochronous Transfer Descriptor), siTD (Split transaction Isochronous Transfer Descriptor), QH (Queue Head), and qTD (Queue element Transfer Descriptor). These descriptors contain information such as maximum packet size, endpoint address, endpoint speed, data flow direction, and buffer positions in system memory etc.

6.2 Isochronous Transfer Descriptor

An iTD is used only for high-speed isochronous endpoints. This always allocated in 16-Dword units to system memory.

6.2.1 Isochronous transfer descriptor format

Table 6-1. Isochronous Transfer Descriptor Format

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00				
Dword0	Next Link Pointer (NLP)			0	TYP	T
Dword1	STA	Transaction 0 Length (T0L)	I	P	Transaction 0 Offset (T0O)
Dword2	STA	Transaction 1 Length (T1L)	I	P	Transaction 1 Offset (T1O)
Dword3	STA	Transaction 2 Length (T2L)	I	P	Transaction 2 Offset (T2O)
Dword4	STA	Transaction 3 Length (T3L)	I	P	Transaction 3 Offset (T3O)
Dword5	STA	Transaction 4 Length (T4L)	I	P	Transaction 4 Offset (T4O)
Dword6	STA	Transaction 5 Length (T5L)	I	P	Transaction 5 Offset (T5O)
Dword7	STA	Transaction 6 Length (T6L)	I	P	Transaction 6 Offset (T6O)
Dword8	STA	Transaction 7 Length (T7L)	I	P	Transaction 7 Offset (T7O)
Dword9	Buffer Pointer (BP Page 0)	EP	0	DA	
Dword10	Buffer Pointer (BP Page 1)	D	MPS		
Dword11	Buffer Pointer (BP Page 2)	0	MLT		
Dword12	Buffer Pointer (BP Page 3)	0			
Dword13	Buffer Pointer (BP Page 4)	0			
Dword14	Buffer Pointer (BP Page 5)	0			
Dword15	Buffer Pointer (BP Page 6)	0			

6.2.2 Isochronous transfer descriptor field definitions

Table 6-2. Description of Isochronous Transfer Descriptors

(1/2)

Name	HC Access	Description
NLP	R	Next Link Pointer This field indicates another Isochronous Transaction descriptor (iTD or siTD) or Queue Head (QH).
TYP	R	QH/(s)iTD/FSTN select This indicates the descriptor type. 00b: iTD 01b: QH 10b: siTD 11b: FSTN
T	R	Terminate 1: Link Pointer field is not valid. 0: Link Pointer field is valid.
STA	R/W	Status Offset Description Definition Bit 3 Active HCD set this bit to a one to enable the execution of this transaction. When the transaction associated with this descriptor is completed, HC sets this bit to a zero. Bit 2 Data buffer Error HC set this bit to a one to indicate overrun or underrun. Bit 1 Babble Detected HC set this bit to a one to indicate that a "babble" is detected. Bit 0 Transaction Error HC set this bit to a one to indicate that transaction error.
TxL	R/W	Transaction X Length For an OUT, this field is the number of data bytes HC will send during an isochronous transaction. HC does not update this field. For an IN, the initial value of the field is the number of bytes HC expects the endpoint to deliver. During the status update, HC writes back the number of bytes successfully received.
I	R	Interrupt On Complete If this bit is set to a one, it specifies that when the transaction completes, HC should issue an interrupt at the next interrupt threshold.
P	R/W	Page Select These bits are set by HCD to indicate which of the buffer page pointers the offset field should be concatenated to produce the starting memory address. For an OUT, these fields may be modified by HC.
TxO	RW	Transaction X Offset This field is a value that is an offset from the beginning of a buffer. For an OUT, these fields may be modified by HC.
BP	R	Buffer Pointer This is a 4K aligned pointer to physical memory.
EP	R	Endpoint Number
DA	R	Device Address

(2/2)

Name	HC Access	Description
D	R	Direction Indicates the data flow direction (IN or OUT) 1: IN 0: OUT
MPS	R	Maximum Packet Size This field indicates the maximum number of bytes (1024 bytes) per data packet that can be received from the endpoint or sent to an endpoint.
MLT	R	Multi This field is used to indicate to HC the number of transactions that should be executed per transaction description. 00b: Reserved 01b: One transaction per transaction description 10b: Two transactions per transaction description 11b: Three transactions per transaction description

6.3 Split Transaction Isochronous Transfer Descriptor

All full-speed isochronous transfers through Transaction Translators are managed using the siTD data structure. This always allocated in 7-Dword units to system memory.

6.3.1 Split transaction isochronous transfer descriptor format

Table 6-3. Split Transaction Isochronous Transfer Descriptor Format

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Dword0	Next Link Pointer (NLP) ... 0 ... TYP ... T
Dword1	D ... PN ... 0 ... HA ... 0 ... EP ... 0 ... DA
Dword2	0 ... UFCM ... UFSM
Dword3	I P ... 0 ... TBT ... CPM ... STA
Dword4	Buffer Pointer (BP Page 0) ... Current Offset (CO)
Dword5	Buffer Pointer (BP Page 1) ... 0 ... TP ... TC
Dword6	Back Pointer (BKP) ... 0 ... T

6.3.2 Split transaction isochronous transfer descriptor field definitions

Table 6-4. Description of Split Transaction Isochronous Transfer Descriptors

(1/2)

Name	HC Access	Description
NLP	R	Next Link Pointer This field indicates another Isochronous Transaction descriptor (iTD or siTD) or Queue Head (QH).
TYP	R	QH/(s)iTD/FSTN select This indicates the descriptor type. 00b: iTD 01b: QH 10b: siTD 11b: FSTN
T	R	Terminate 1: Link Pointer field or Back Pointer field is not valid. 0: Link Pointer field or Back Pointer field is valid.
D	R	Direction Indicates the data flow direction (IN or OUT) 1: IN 0: OUT
PN	R	Port Number This field indicates the port number of the recipient transaction translator.
HA	R	Hub Address This field holds the device address of the transaction translator's hub.
EP	R	Endpoint Number
DA	R	Device Address
UFCM	R	Split Completion Mask (μFrame C-mask) This field are used to determine during which micro-frames HC should execute complete-split transactions.

(2/2)

Name	HC Access	Description
UFSM	R	Split Start Mask (μFrame C-mask) This field are used to determine during which micro-frames HC should execute start-split transactions.
I	R	Interrupt On Complete If this bit is set to a one, it specifies that when the transaction completes, HC should issue an interrupt at the next interrupt threshold.
P	R/W	Page Select Used to indicate which data page pointer should be concatenated with the CO to construct a data buffer pointer.
TBT	R/W	Total Bytes to Transfer HCD initiates this field with the total number of bytes expected in this transfer.
CPM	R/W	μFrame Complete-split Progress Mask This field is used by HC to record which split-completes has been executed.
STA	R/W	Status Offset Description Definition Bit 7 Active HCD set this bit to a one to enable the execution of this transaction. Bit 6 ERR HC set this bit to a one when an ERR response is received from the transaction translator. Bit 5 Data buffer Error HC set this bit to a one to indicate overrun or underrun. Bit 4 Babble Detected HC set this bit to a one to indicate that a "babble" is detected. Bit 3 Transaction Error HC set this bit to a one to indicate that transaction error. Bit 2 Missed μFrame miss a required complete-split transaction. Bit 1 SplitXstate 0: Do start split 1: Do complete split Bit 0 reserved
BP	R	Buffer Pointer This is a 4K aligned pointer to physical memory.
CO	R/W	Current offset This field is a value that is an offset from the beginning of a buffer.
TP	R/W	Transaction position 00b: All 01b: Begin 10b: Mid. 11b: End.
TC	R/W	Transaction count HCD initiates this field with the number of OUT start-splits this transfer requires.
BKP	R	siTD Back Pointer This is a physical memory pointer to an siTD.

6.4 Queue Element Transfer Descriptor

This data structure is only used with queue head. This structure can describe one or more USB transaction. This structure is 32 bytes (or one 32-byte cache line).

6.4.1 Queue element transfer descriptor format

Table 6-5. Queue Element Transfer Descriptor Format

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00			
Dword0	Next qTD Pointer (NTP)		0	T
Dword1	Alternate Next qTD Pointer (ANTP)		0	T
Dword2	G | TBT | I | CP | EC | PID | STA			
Dword3	Buffer Pointer (BP Page 0)	Current Offset (CO)		
Dword4	Buffer Pointer (BP Page 1)	0		
Dword5	Buffer Pointer (BP Page 2)	0		
Dword6	Buffer Pointer (BP Page 3)	0		
Dword7	Buffer Pointer (BP Page 4)	0		

6.4.2 Queue element transfer descriptor field definitions

Table 6-6. Description of Queue Element Transfer Descriptors

(1/2)

Name	HC Access	Description
NTP	R	Next Element Transaction Descriptor Link Pointer This field indicates next Queue element Transaction descriptor.
ANTP	R	Alternate Next Element Transaction Descriptor Link Pointer This field contains the physical memory address of the next qTD to be processed in the event that the current qTD execution encounters a short packet.
T	R	Terminate 1: Pointer field is not valid. 0: Pointer field is valid.
G	R/W	Data Toggle This is data toggle sequence bit.
TBT	R/W	Total Bytes to Transfer HCD initiates this field with the total number of bytes expected in this transfer.
I	R	Interrupt On Complete If this bit is set to a one, it specifies that when the transaction completes, HC should issue an interrupt at the next interrupt threshold.
CP	R/W	Current Page This field is used as an index into the qTD buffer pointer list.
EC	R/W	Error Counter This is a 2 bit down counter. When HC find transaction error, HC decreases this field.
PID	R	PID Code 00: OUT 01: IN 10: SETUP 11: Reserved

(2/2)

Name	HC Access	Description		
STA	R/W	Status		
		Offset	Description	Definition
		Bit 7	Active	HCD set this bit to a one to enable the execution of this transaction.
		Bit 6	Halted	HC set this bit to a one when a serious error has occurred at the device/endpoint address.
		Bit 5	Data buffer Error	HC set this bit to a one to indicate overrun or underrun.
		Bit 4	Babble Detected	HC set this bit to a one to indicate that a "babble" is detected.
		Bit 3	Transaction Error	HC set this bit to a one to indicate that transaction error.
		Bit 2	Missed μFrame	see specification.
		Bit 1	SplitXstate	0: Do start split 1: Do complete split
		Bit 0	Ping State	0: Do OUT 1: Do PING
BP	R	Buffer Pointer This is a 4K aligned pointer to physical memory.		
CO	R/W	Current offset This field is a value that is an offset from the beginning of a buffer.		

6.5 Queue Head

This data structure is only used with queue head. This structure can describe one or more USB transaction. This structure is 32 bytes (or one 32-byte cache line).

6.5.1 Queue head format

Table 6-7. Queue Head Format

	31–08	07–03	02	01	00
Dword0	Queue Head Horizontal Link pointer (QHP)		0	TYP	T

	31–28	27	26	25–16	15	14	13–12	11–08	07	06–00
Dword1	RL	C		MPS	H	X	EPS	EP	I	DA

	31–30	29–23	22–16	15–08	07–00
Dword2	MLT	PN	HA	UFCM	UFSM

	31–05	04–00
Dword3	Current qTD Pointer (CTP)	0

	31–05	04–01	00
Dword4	Next qTD Pointer (NTP)	0	T
Dword5	Alternate Next qTD Pointer (ANTP)	NC	T

	31	30–16	15	14–12	11–10	09–08	07–00
Dword6	G	TBT	I	CP	EC	PID	STA

	31–12	11–00
Dword7	Buffer Pointer (BP Page 0)	Current Offset (CO)

	31–12	11–08	07–00
Dword8	Buffer Pointer (BP Page 1)	0	CPM

	31–12	11–05	04–00
Dword9	Buffer Pointer (BP Page 2)	SB	FT

	31–12	11–00
Dword10	Buffer Pointer (BP Page 3)	0
Dword11	Buffer Pointer (BP Page 4)	0

6.5.2 Queue head field definitions

Table 6-8. Description of Queue Head

(1/2)

Name	HC Access	Description
QHP	R	Queue Head Horizontal Link Pointer This field indicates another Queue Head (QH).
TYP	R	QH/(s)iTD/FSTN select This indicates the descriptor type. 00b: iTD 01b: QH 10b: siTD 11b: FSTN
T	R	Terminate 1: Pointer field is not valid. 0: Pointer field is valid.
RL	R	Nak Count Reload This field contains a value, which is used by HC to reload the Nak Counter field.
C	R	Control Endpoint Flag HCD set this bit to a one to indicate the endpoint is not a high-speed device, and the endpoint is a control endpoint.
MPS	R	Maximum Packet Size This field indicates the maximum number of bytes (1024 bytes) per data packet that can be received from the endpoint or sent to an endpoint.
H	R	Head of Reclamation List Flag HCD set this bit to a one to mark a queue head as being the head of the reclamation list.

(2/2)

Name	HC Access	Description
X	R	Data Toggle Control 0b: Ignore G bit from incoming qTD. HC preserves DT bit in QH. 1b: Initial data toggle comes from incoming qTD G bit.
EPS	R	Endpoint Speed 00b: Full-speed 01b: Low-speed 10b: High-speed 11b: Reserved
EP	R	Endpoint Number
I	R	Inactive on Next Transaction This bit is set only when the queue head is in the Periodic Schedule and the EPS field indicates Full- or Low-speed.
DA	R	Device Address
MLT	R	Multi This field is used to indicate to HC the number of transactions that should be executed per transaction description. 00b: Reserved 01b: One transaction per transaction description 10b: Two transactions per transaction description 11b: Three transactions per transaction description
PN	R	Port Number This field indicates the port number of the recipient transaction translator.
HA	R	Hub Address This field holds the device address of the transaction translator's hub.
UFCM	R	Split Completion Mask (μFrame C-mask) This field are used to determine during which micro-frames HC should execute complete-split transactions.
UFSM	R	Split Start Mask (μFrame C-mask) This field are used to determine during which micro-frames HC should execute start-split transactions.
CTP	R	Current Element Transaction Descriptor Link Pointer This field indicates current Queue element Transaction descriptor.
NC	R/W	Nak counter This is a counter HC decrements whenever a transaction results in a Nak or Nyet response.
CPM	R/W	μFrame Complete-split Progress Mask This field is used to track the progress of a interrupt split-transaction.
FT	R/W	Split-transaction Frame Tag This field is used to track the progress of a interrupt split-transaction.
SB	R/W	S-byte This field is used to keep track of the number of bytes sent or received during a IN or OUT split-transaction.

6.6 Periodic Frame Span Traversal Node (FSTN)

This data structure is only used for Full- Low-speed transaction that spans a Host-frame boundary.

6.6.1 Periodic frame span traversal node descriptor format

Table 6-9. Queue Head Format

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03	02 01	00
Dword0	Normal Path Link Pointer	0 TYP	T
Dword1	Back Path Link Pointer	0 TYP	T

6.6.2 Periodic frame span traversal node field definitions

Table 6-10. Description of Queue Head

Name	HC Access	Description
NPLP	R	Normal Path Link Pointer This field contains the address of the next data to be processed in the periodic list.
TYP	R	QH/(s)iTD/FSTN select This indicates the descriptor type. 00b: iTD 01b: QH 10b: siTD 11b: FSTN
T	R	Terminate 1: Pointer field is not valid. 0: Pointer field is valid.
BPLP	R	Back Path Link Pointer This field contains the address of Queue Head.
TYP	R	Must be set to indicate Queue Head.
T	R	Terminate 1: Pointer field is not valid. 0: Pointer field is valid.

CHAPTER 7 POWER MANAGEMENT

The μPD720101 supports some power management functions.

1. Compliant with PCI Bus Power Management Interface Specification (Rev 1.1)
2. Support PCI CLKRUN# signal
3. Support special clock stopping operation to minimize the power consumption. ,etc

This chapter describes the power management.

7.1 Bus Power States and Function Power Management States

This section defines the PCI Bus Power States, USB Bus States, and PCI Function Power Management States.

7.1.1 PCI bus power states

B0 : Vcc = On, PCLK = 33 MHz, PCI Bus activity = any PCI transaction, interrupt, or PME (Power Management Event) event. A system reset always returns the PCI bus to B0. Also, CLKRUN function is included this state. For detail about CLKRUN, see **PCI Mobile Design Guide Version1.1**.

B1 : Vcc = On, PCLK = 33 MHz, PCI Bus activity = PME event, State of PCI Bus is a perpetual idle. All PCI bus signals are required to be held at valid logic states at all time. Bus parking is allowed.

B2 : Vcc = On, PCLK = Stopped and held in the low state, PCI Bus activity = PME event. All PCI bus signals are required to be held at valid logic states at all time. Bus parking is allowed.

B3 : Vcc = Off, PCLK = N/A, PCI Bus activity = PME event

7.1.2 USB bus states

USB_Reset : USB Bus = Reset, stopped USB bus activity

USB_Operational : USB Bus = Active

USB_Suspend : USB Bus = Suspend, Constant J state

USB_Resume : USB Bus = Resume, K state

7.1.3 PCI function power management states

The μPD720101 has three host controller cores (OHCI#1, OHCI#2, EHCI). Each host controller core has the power management registers, which comply with PCI Bus Power Management Interface Specification (Rev 1.1), respectively. However, It is illogical to put each host controller core into different PCI Function Power Management States. Same value shall be written to the power management registers of three host controller cores.

D0 : Normal operation state.

During this state, PCI Bus Power State should be "B0" and PCI "CLK" is just 33 MHz. And then PCI side can use any PCI transaction which is used by host controller core, interrupt, and PME event. On the other hand, the host controller core is put into one of following USB Bus States (USB_Reset, USB_Operational, USB_Suspend, or USB_Resume).

D1 : Light sleep state.

During this state, PCI Bus Power State should be either "B0" or "B1". PCI "CLK" is just 33MHz. If PCI Bus Power State is "B1", host controller core will be allowed only PME event. For USB side, the host controller core is put into one of following USB Bus States (USB_Reset, USB_Suspend).

D2 : Sleep state.

During this state, PCI Bus Power State can be put into "B0", "B1", or "B2". If PCI Bus Power State is "B1" or "B2", OHCI host controller core will be allowed only PME event. For USB side, the host controller core is put into one of following USB Bus States (USB_Reset, USB_Suspend).

D3$_{hot}$: Disable state.

During this state, PCI Bus Power State can be put into "B0", "B1", or "B2". If PCI Bus Power State is "B1" or "B2", OHCI host controller core will be allowed only PME event. For USB side, the host controller core is put into one of following USB Bus States (USB_Reset, USB_Suspend).

D3$_{cold}$: Power-off state.

During this state, PCI Bus Power State should be "B3" and the host controller core can be allowed Bus segment reset or PME event. For USB side, the host controller core should put into one of following USB Bus States (USB_Reset, USB_Suspend).

7.2 Power Management Event

As above mentioned, the host controller core can use PME (Power Management Event) event during all PCI Bus Power States. The PME event can be indicated by PME0 (Power Management Event) signal. And it is used to indicate that host controller core's power state should be changed. The following sections describe PME event.

7.2.1 PME event support

If the power state of host controller core should be changed from D0, D1, D2, or D3$_{hot}$ to the other, PME event will be occurred as shown in the PME_support bits in PMC (Power Management Capabilities) register. For default setting, the host controller core does not support the wake up event detection under D3$_{cold}$. If wake up event detection under D3$_{cold}$ support is required, bit 15 of PME_support in PMC register shall be set "high" and the Aux_Current bits in PMC register should also be set to appropriate value. The PME_support and Aux_Current can be written by BIOS when ID_Write_Enable in EHCI's (OHCI #1's) configuration space is set to "1" or can be loaded from external serial ROM with I^{2}C I/F before starting PCI configuration registers access if serial ROM is available. When the system boot or the resuming sequence from power-off state is occurred, these bits should be restored if the host controller core supports the wake up event detection under D3$_{cold}$. When these bits are set, all three host controller cores (OHCI#1, OHCI#2, EHCI) should be set to same appropriate value.

7.2.2 How to support the transition from D3$_{cold}$ to D0

If the wake up event detection under D3$_{cold}$ support is required, not only the setting for the related register shall be considered, butsystem board implementation shall be taken into consideration too.

If the wake up event detection under D3$_{cold}$ support is required, the host controller cores will be put into D3$_{cold}$ when system will go to S3. And the system SW may set Power State and PME_En bits to appropriate value before S3 transition. When system is in S3 and the device is in D3$_{cold}$, PCI Bus is not powered (B3 state) because main power is shut down. When wake up event is occurred, PME0 is asserted without PCI CLK.

This device does not provide 3.3Vaux pin which is power supply to realize PME0 generation under D3$_{cold}$. If PME0 generation under D3$_{cold}$ support is required, auxiliary power source instead of system main power supply V$_{CC}$, which supplies power to this device's V$_{DD}$ for S3 system sate, should be required on system board implementation.

Also if PME0 generation under D3cold support is required, reset and I/O buffer enable signals shall be connected as below.

Pin name	Support PME0 generation under D3cold	Not support PME0 generation under D3cold
VBBRST0	Connects to system reset signal as RSMRST#.	Connects to PCI "RST#" signal.
VCCRST0	Connects to PCI "RST#" signal. **Note**	"H" clamp
V_{DD}	Should be changed backup power supply under suspend mode.	Connects to system main power supply.
V_{DD_PCI}	Connect PCI bus power or V_{DD}.	Connect PCI bus power or V_{DD}.
USB_VBUS	Should be changed backup power supply under suspend mode.	Connects to system main power supply.

Note Under D3cold, these pins should be clamped at low level.

VCCRST0 is a signal to set Power State bits to D0 from D3. When the device is in D3, Only Power State bits are reset by the rising edge of VCCRST0. On the other hand, When the device is not in D3, VCCRST0 clears all circuit in this device. VCCRST0 also controls enable or disable PCI Bus signal. It is useful to avoid some noise such as invalid PCI write access on the PCI Bus under D3cold.

VCCRST0 should be controlled as follows.

1) VCCRST0 should be set to "high" to support Normal PCI Operation.
2) If the transition from D3cold to D0 support is required, VCCRST0 should be set to "low" to disable all PCI accesses before system goes to S3 state (Suspended with PCI B3 state) when PCI Bus is in B3 (PCI Power off).
3) When PCI Bus wakes up from B3, VCCRST0 should be set to "high" after PCI Bus state transitions to B0 (after PCI RST# is deasserted). Also, When the device wakes up from D3cold by system (exp. Triggered by Other device wake up interrupt), VCCRST0 should be set to "high" as same timing.

If the transition from D3cold to D0 support is not required, VCCRST0 is always tied to V_{DD} bus line.

Figure 7-1. Wake Up State Transition from D3$_{cold}$ (Using 30-MHz X'tal)

* System clock : is generated by internal OCS block with external X'tal.
* Analog PLL output : is generated by analog PLL. The clocks for internal logic and PLL output are active under D0.
* PCI clock in this device is running independently of internal oscillator block output.

(A) : PLL stops in the following condition.
　　　　　(PCI_Power_State = ! (D0 state for all of HC macros))
　　　　　& (USBSTS_HcHalt bit is set 1 for HS-HC macro)
　　　　　& (Set HCControl_HCFS = "USB_Reset or USB_Suspend" for CL-HD 1, 2 macros)
　　　　　& (All ports are suspended or disabled regardless of port owner)

(B) : VCCRST0 becomes "L" and system clock is disable.

(C) : VCCRST0 becomes "H" and system clock is enable.

　　　** If the device's status is changed by the wake up event, PLL may start running even if VCCRST0 is not set to high.

(D) : One of the condition noted in (A) is cleared, and PLL output resume within 30 μs.

Figure 7-2. Wake Up State Transition from D3cold (Using 48-MHz Oscillator)

* System clock : is generated by external oscillator block with external oscillator.
* Analog PLL output : is generated by analog PLL. The clocks for internal logic and PLL output are active under D0.
* PCI clock in this device is running independently of internal oscillator block output.

(A) : System sets HS-HC to "Run" state (HcHalted bit = 0).
(B) : After PLL is locked, PLL starts to output 60 MHz clock.
(C) : PLL stops in the following condition.
        (HcHalted bit of HS-HC is set to "1") & (HS-HC is idle) & (Port Owner is EHCI and not in Reset/Resume sequence)
(D) : System sets all Power state bits of HC macros (HS-HC, CL-HC1, 2) to NOT D0 state.
(E) : VCCRST0 becomes "L", but external oscillator must be valid.
(F) : VCCRST0 becomes "H".
       ** If the device's status is changed by the wake up event, PLL may start running even if VCCRST0 is not set to high.
(G) : One of the condition noted in (C) is cleared, and PLL output resume within 30 μs.

7.2.3 PME0 assertion

The Power Management Event signal (PME0) of this device is OR-ed signal of the value of PME_Status bit in PMECSR register, which is the part of power management registers. The power management registers, which comply with PCI Bus Power Management Interface Specification (Rev 1.1), are provided by three host controller cores (OHCI#1, OHCI#2, EHCI) respectively and are allocated in configuration space. Each PME_Status bit is set by wake up event which is allowed for each port.

- When the port is controlled by OHCI #1 or OHCI #2, the following setting should be done to reflect PME event detection on PME_Status bit. If the device connect/disconnect detection is wake up event, DRWE bit in HcRhStatus reg. and RWE bit in HcControl reg. of related OHCI host controller should be set to "high".

- If the resume signaling (remote wake up event) from connected device is wake up event, RWE bit in HcControl reg. of related OHCI host controller should be set to "high".

When the port is controlled by EHCI, the following setting should be done to reflect PME event detection on PME_Status bit.

- If the device connect detection is wake up event, WKCNNT_E bit in PORTSCn reg. should be set to "high".

- If the device disconnect detection is wake up event, WKDSCNNT_E bit in PORTSCn reg. should be set to "high".

- If the over current detection is wake up event, WKOC_E bit in PORTSCn reg. should be set to "high".

When PME_En bit in PMECSR register is set to "high", the value of related PME_Status bit is appeared at PME0 pin. The assertion and deassertion of PME0 signal is not synchronized with PCI "CLK" (PCLK). So, even if PCLK is stopped, this device can assert PME0 signal. It is possible to generate PME0 signal under D0, D1, D2, D3$_{hot}$, and D3$_{cold}$ (by special setting).

After above setting, PME0 signal will be asserted if wake up event is detected.

D0 : Normal operation state.

USB = USB_Suspend, the port is controlled by OHCI #1 or #2. :

For PME0 assertion

Action	RWE bit	DRWE bit	PME_En bit	PME0
Device connect	0	X	X	Disable
	1	0	X	Disable
	1	X	0	Disable
	1	1	1	Enable
Device disconnect	0	X	X	Disable
	1	0	X	Disable
	1	X	0	Disable
	1	1	1	Enable
Remote wake up	0	X	X	Disable
	1	X	0	Disable
	1	X	1	Enable

For Interrupt assertion

Action	DRWE bit	RD bit	RHSC bit	Interrupt
Device connect	0	X	0	Disable
	0	X	1	Enable
	1	0	0	Disable
	1	X	1	Enable
	1	1	X	Enable
Device disconnect	0	X	0	Disable
	0	X	1	Enable
	1	0	0	Disable
	1	X	1	Enable
	1	1	X	Enable
Remote wake up	X	0	X	Disable
	X	1	X	Enable

Remarks 1. RD bit is located in HcInterruptEnable Reg.

2. RHSC bit is located in HcInterruptEnable Reg.

3. If device disconnect event is occurred under RWE = DRWE = PME_EN = 1 and RD or RHSC = 1, PME0 and interrupt will be asserted at the same time.

4. After wake up event is detected, even if RWE and DRWE are set "high", PME0/interrupt will not be asserted by latest wake up event. On the other hand, if PME_En, RD, and RHSC are set "high" after wake up event is detected, PME0/interrupt will be asserted by latest wake up event.

USB = USB_Suspend (Port suspend), the port is controlled by EHCI. :
For PME0 assertion

Action	WKCNNT_E bit	WKDSCNNT_E bit	WKOC_E bit	PME_En bit	PME0
Device connect	0	X	X	X	Disable
	1	X	X	0	Disable
	1	X	X	1	Enable
Device disconnect	X	0	X	X	Disable
	X	1	X	0	Disable
	X	1	X	1	Enable
Remote wake up	X	X	X	0	Disable
	X	X	X	1	Enable
Over current	X	X	0	X	Disable
	X	X	1	0	Disable
	X	X	1	1	Enable

For Interrupt assertion

Action	Port Change Interrupt Enable bit	Interrupt
Device connect	0	Disable
	1	Enable
Device disconnect	0	Disable
	1	Enable
Remote wake up	0	Disable
	1	Enable
Over current	0	Disable
	1	Enable

Remarks 1. Port Change Interrupt Enable (PCIE) bit is located in USBINTR Reg.
2. If device disconnect event is occurred under WKDSCNNT_E = PME_EN = PCIE = 1, PME0 and interrupt will be asserted at the same time.
3. After related wake up event is detected, even if WKCNNT_E, WKDSCNNT_E or WKOC_E are set "high", PME0 will not be asserted by latest wake up event. On the other hand, if PME_En and PCIE are set "high" after wake up event is detected, PME0/interrupt will be asserted by latest wake up event.

USB = USB_Reset, the port is controlled by OHCI #1, #2 :

Host controller core cannot detect the device connect, device disconnect, remote wake up event. It detects only over current issue.

USB = USB_Reset (Port Reset), the port is controlled by EHCI. :

Host controller core cannot detect the device disconnect, remote wake up event. Also, the device connect is not detected because the device is connected to port under Port Reset. It detects only over current issue.

D1 : Light sleep state, D2 : Sleep state, D3$_{hot}$ or D3$_{cold}$: Disable state.

USB = USB_Suspend/USB_Reset, the port is controlled by OHCI #1 or #2. :

For PME0 assertion

Action	RWE bit	DRWE bit	PME_EN bit	PME0
Device connect	0	X	X	Disable
	1	0	X	Disable
	1	X	0	Disable
	1	1	1	Enable
Device disconnect	0	X	X	Disable
	1	0	X	Disable
	1	X	0	Disable
	1	1	1	Enable
Remote wake up	0	X	X	Disable
	1	X	0	Disable
	1	X	1	Enable

Remark After wake up event is detected, even if RWE and DRWE are set "high", PME0 will not be asserted by latest wake up event. On the other hand, if PME_En is set "high" after wake up event is detected, PME0 will be asserted by latest wake up event.

For Interrupt assertion
Not available under these device state

USB = USB_Suspend (Port suspend), the port is controlled by EHCI. :

For PME0 assertion

Action	WKCNNT_E bit	WKDSCNNT_E bit	WKOC_E bit	PME_EN bit	PME0
Device connect	0	X	X	X	Disable
	1	X	X	0	Disable
	1	X	X	1	Enable
Device disconnect	X	0	X	X	Disable
	X	1	X	0	Disable
	X	1	X	1	Enable
Remote wake up	X	X	X	0	Disable
	X	X	X	1	Enable
Over current	X	X	0	X	Disable
	X	X	1	0	Disable
	X	X	1	1	Enable

Remark After related wake up event is detected, even if WKCNNT_E, WKDSCNNT_E or WKOC_E are set "high", PME0 will not be asserted by latest wake up event. On the other hand, if PME_En is set "high" after wake up event is detected, PME0 will be asserted by latest wake up event.

For Interrupt assertion
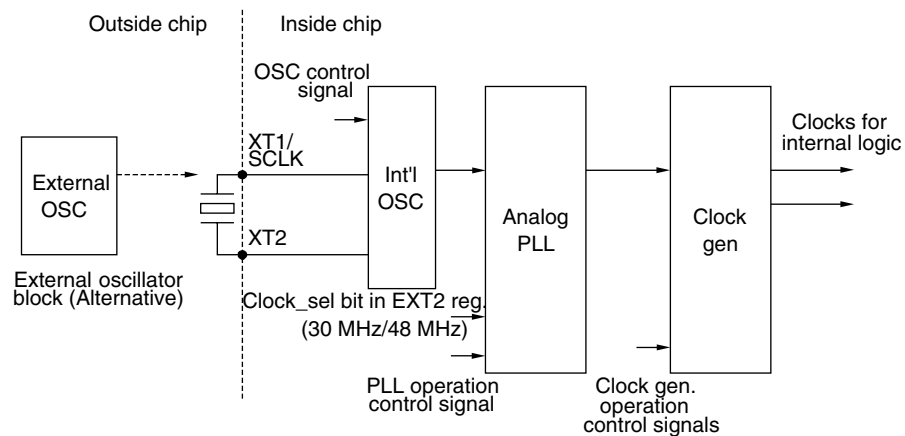Not available under these device state

7.3 Control for System Clock Operation

When host controller core is put into power down state as D1, D2 and D3hot, clock system is controlled to reduce power consumption. This section describes the clock system and the power management for clock path.

7.3.1 Clock system

The μPD720101 uses 30 MHz X'tal or 48 MHz oscillator block for system clock signal. System clock frequency is selected by "Clock_sel bit" in EXT2 register. Internal Analog PLL generates the internal system clock signals, which supply to logic circuit. Internal system clock signals can be controlled to stop and run by μPD720101 itself. So if 48 MHz oscillator block is used, 48 MHz Oscillator block should be always active. PCI clock is independent of system clock and it is used for only PCI related logic to realize power management control circuit. Figure 7-3 shows μPD720101's clock system without PCI Clock.

Figure 7-3. μPD720101's Clock System

7.3.2 Condition for clock system stopping/resuming

There are 3 levels of clock stopping to minimize power consumption of the chip. Lower level is that the clocks for internal logic are stopped. Middle level is that the clocks for internal logic and Analog PLL are stopped. Higher level is that all clock signals, which include internal oscillator block output, are stopped completely.

At first, the following condition should be satisfied to stop clock function.

1) HcHalted bit in USBSTS reg. for EHCI should be set to "high".

2) Suspend bit in PORTSCn register should be set to "high" or Port Enabled/Disabled bit in PORTSCn register should be set to "low". This means that all ports should be put into suspend or disabled.

3) HCFS bit in HcControl reg. should be set to "USB_Suspend" or "USB_Reset".

And then OCHI is in USB_Suspend or USB_Reset state under D1, D2, D3hot, and D3cold. On the other hand, EHCI is in USB_Suspend (per Port) state under D1, D2, D3hot, and D3cold

a. **And also, if following condition is satisfied, the clocks for internal logic are stopped.**

1) VCCRST should be set to "high".

2) All PCI Function Power Management States of 3 host controller cores are D0 sate.

b. **And also, if following condition is satisfied, the clocks for internal logic and Analog PLL are stopped.**

1) VCCRST should be set to "high".

2) All PCI Function Power Management States of 3 host controller cores are not D0 sate.

c. And also, if following condition is satisfied, the internal oscillator block output is stopped.
   1) VCCRST should be set to "low".
   2) All PCI Function Power Management States of 3 host controller cores are not D0 sate.

When one of following condition is satisfied, the internal oscillator block out restarts.
   1) System should be changed the setting as above mentioned.
   2) There is any bus activity (Remote wake up signaling, connect/disconnect at the port which is controlled by OHCI #1 or #2) on USB Bus line.
   3) When connect/disconnect/over current detection is allowed as wake up event, there is connect/disconnect/over current detection at the port, which is controlled by EHCI.

Figure 7-4. Clock Operation Diagram (Using 30-MHz X'tal)

(W1) : Wake up event causes all internal clocks rerunning and asserts PME0 after wake up event is checked.
(W2) : After the chipset on system receives PME0, the system starts wake up sequencing. The chipset wakes system power supply and clock generator up. And then, system main power supply is activated and system PCI bus transitions from B3 to B0.
(W3) : When the device find the rising edge of VCCRST0, Power_State bit in Power Management Control/Status (PMCSR) transitions from D3 to D0. And at the same time HC accepts PCI bus access.
(W4) : System SW (BIOS) checks each PME_Status register for 3 host controller cores in the device via PCI configuration access.

Figure 7-5. Clock Operation Diagram (Using 48-MHz Oscillator)

(W1) : Wake up event causes all internal clocks rerunning and asserts PME0 after wake up event is checked.
(W2) : After the chipset on system receives PME0, the system starts wake up sequencing. The chipset wakes system power supply and clock generator up. And then, system main power supply is activated and system PCI bus transitions from B3 to B0.
(W3) : When the device find the rising edge of VCCRST0, Power_State bit in Power Management Control/Status (PMCSR) transitions from D3 to D0. And at the same time HC accepts PCI bus access.
(W4) : System SW (BIOS) checks each PME_Status register for 3 host controller cores in the device via PCI configuration access.

Note : HC activates analog PLL only when HcHalted bit of USBSTS register of HS-HC is "0".
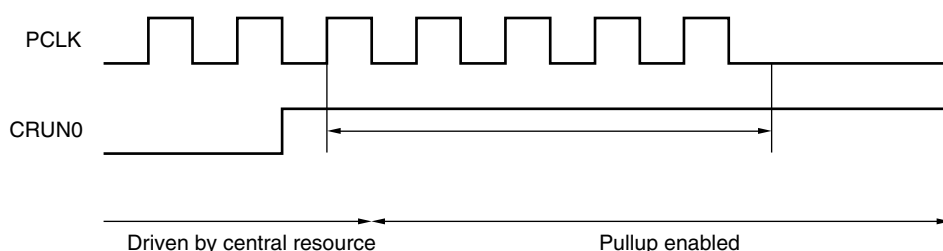
7.3.3 CLKRUN# support

This host controller supports CLKRUN# signal. And then HC can stop PCI clock when HC does not need PCI clock to work. This section describes CLKRUN# signals.

The HC can stop PCI clock except for following condition.

- OHCI host controller core needs to work as PCI bus master function.
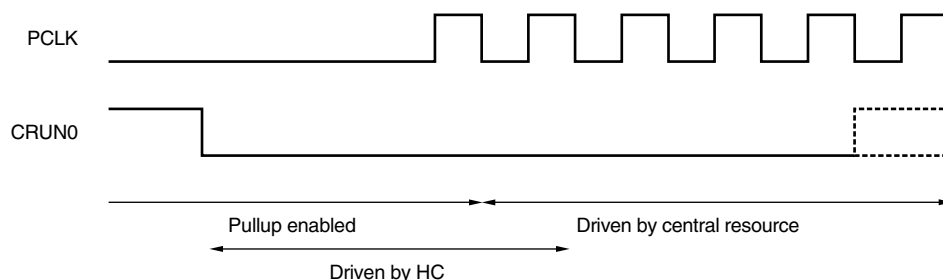- USBCMD register's RS bit in EHCI host controller is set to "high".

Figure 7-6 shows PCI clock stop sequence and Figure 7-7 shows PCI clock start sequence.

Figure 7-6. PCI Clock Stop

After CRUN0 is deasserted, PCLK continues to run for a minimum of 4 clock period.
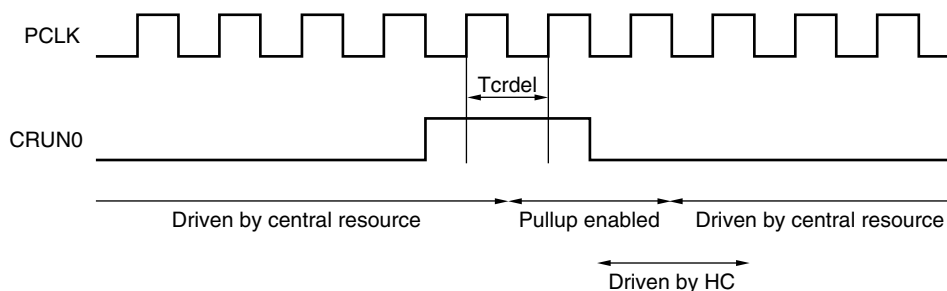
Figure 7-7. PCI Clock Start

HC asserts CRUN0 asynchronously and it holds CRUN0 asserted until it detects two rising edge of PCLK. After the second clock edge, HC disables its open drain buffer. The central resource drives CRUN0 low at any time after it detects that the line asserted by HC, but not later than on 3rd clock. It also must not drive CRUN0 high earlier than on 5th clock.

HC may require the PCI clock to be active for completing some internal processes. At that time, HC will assert CRUN0 after it has been deasserted for two successive clocks.

Figure 7-8. Maintaining PCI Clock

	Min.	Max.
Tcrdel	1 clock	2 clocks

The HC asserts CRUN0 within a certain time window (Tcrdel). HC holds CRUN0 asserted until it detects two rising edge of PLCK. After the second clock edge, the HC must disable its open drain driver.

CHAPTER 8 HOW TO WRITE EXTERNAL SERIAL ROM

In this host controller, some fields such as subsystem ID in PCI configuration registers are programmable. The host controller has I²C interface to hold the 24 bytes customer specific value for PCI configuration registers on external serial ROM. This chapter describes how to use external serial ROM interface.

8.1 Registers to Control I²C Interface

The three registers, which are allocated in EHCI's operational register space, are used to control I²C Interface. And then, Ehci_mask bit (in EXT2 register) in OHCI#1 PCI configuration space should be set to a zero to enable EHCI's operational register space if I²C interface. These registers are write-only. When these registers are read, it returns 00h.

Register: I2C_CMD   **Offset Address: F4h**

Field	Bit	Read/Write HCD	Value (Default)	Comment
Page Write Command (PWC)	0	W	Undefined	1: Issue page_write command to external serial ROM. 0: Issue sequential_read command to external serial ROM.
Page for Page Write	2 : 1	W	Undefined	00: When PWC = 1, Page_0 page_write command will be issued. 01: When PWC = 1, Page_1 page_write command will be issued. 10: When PWC = 1, Page_2 page_write command will be issued. 11: When PWC = 0, sequential_read command will be issued.
Reserved	31 : 3	NA	Undefined	Reserved

Register: I2C_WND0   **Offset Address: F8h**

Field	Bit	Read/Write HCD	Value (Default)	Comment
Window0	31 : 0	W	Undefined	Lower Dword temporarily register for page_write to external serial ROM. This register should be written as Dword.

Register: I2C_WND1   **Offset Address: FCh**

Field	Bit	Read/Write HCD	Value (Default)	Comment
Window1	31 : 0	W	Undefined	Upper Dword temporarily register for page_write to external serial ROM. This register should be written as Dword.

8.2 Supported Command for I²C Interface

The I²C interface of HC supports only 8 bytes mode page_write and sequential_read command. When programming external serial ROM for the first time, 3 page_write commands shall be issued to hold all 24 bytes customer specific value for PCI configuration registers. When partial data is required to be updated in serial ROM, page (8 bytes) boundary shall be written. Note that Serial ROM can not be used with I²C, which does not support 8 bytes mode page_write command. Table 8-1 shows the semantics for each byte or bit in each page.

Table 8-1. Semantics for Each Byte/Bit in Page

(1/2)

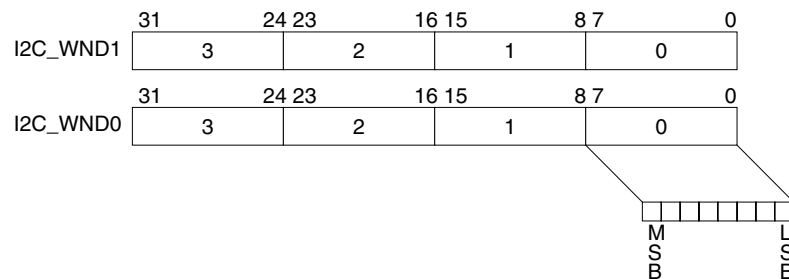| Page	Byte No.	Semantics	Default Value	Window
Page_0	0	Lower byte of Subsystem Vender ID for OHCI #1	33h	I2C_WND0
Page_0	1	Upper byte of Subsystem Vender ID for OHCI #1	10h	
Page_0	2	Lower byte of Subsystem Vender ID for OHCI #2	33h	
Page_0	3	Upper byte of Subsystem Vender ID for OHCI #2	10h	
Page_0	0	Lower byte of Subsystem Vender ID for EHCI	33h	I2C_WND1
Page_0	1	Upper byte of Subsystem Vender ID for EHCI	10h	
Page_0	2	Lower byte of Subsystem ID for OHCI #1	35h	
Page_0	3	Upper byte of Subsystem ID for OHCI #1	00h	
Page_1	0	Lower byte of Subsystem ID for OHCI #2	35h	I2C_WND0
Page_1	1	Upper byte of Subsystem ID for OHCI #2	00h	
Page_1	2	Lower byte of Subsystem ID for EHCI	E0h	
Page_1	3	Upper byte of Subsystem ID for EHCI	00h	
Page_1	0	Min_Gnt for OHCI #1	01h	I2C_WND1
Page_1	1	Min_Gnt for OHCI #2	01h	
Page_1	2	Min_Gnt for EHCI	10h	
Page_1	3	Max_Lat for OHCI #1	2Ah	
Page_2	0	Max_Lat for OHCI #2	2Ah	I2C_WND0
Page_2	1	Max_Lat for EHCI	22h	
Page_2	2 (bit2:0)	Aux_Current for OHCI #2	000b	
Page_2	2 (bit3)	PME_support for OHCI #2	0b	
Page_2	2 (bit6:4)	Aux_Current for OHCI #1	000b	
Page_2	2 (bit7)	PME_support for OHCI #1	0b	
Page_2	3 (bit2:0)	Aux_Current for EHCI	000b	
Page_2	3 (bit3)	PME_support for EHCI	0b	
Page_2	3 (bit7:4)	NEC private #10 (Should write default value.)	0000b	
Page_2	0 (bit0)	NEC private #7 (Should write default value.)	0b	I2C_WND1
Page_2	0 (bit1)	PPC_setting in EXT1 register	1b	
Page_2	0 (bit2)	NEC private #3 (Should write default value.)	0b	
Page_2	0 (bit3)	NEC private #2 (Should write default value.)	0b	
Page_2	0 (bit4)	NEC private #1 (Should write default value.)	0b	

(2/2)

Page	Byte No.	Semantics	Default Value	Window
Page_2	0 (bit7:5)	Port No in EXT1 register	101b [Note]	I2C_WND1
Page_2	1 (bit3:0)	NEC private #4 (Should write default value.)	0011b	
Page_2	1 (bit7:4)	NEC private #5 (Should write default value.)	0011b	
Page_2	2 (bit4:0)	NEC private #6 (Should write default value.)	10000b	
Page_2	2 (bit5)	Legc_mode in EXT1 register	0b	
Page_2	2 (bit6)	Clock select in EXT2 register	0b	
Page_2	2 (bit7)	Ehci_mask in EXT2 register	0b	
Page_2	3	NEC private #8 (Should write default value.)	6Ch	

Note Prohibited setting the value except for 2h - 5h.

The default value in table shows the initiated value of register in HC without external serial ROM. NEC private bytes or bits should write as default value when external serial ROM is used.
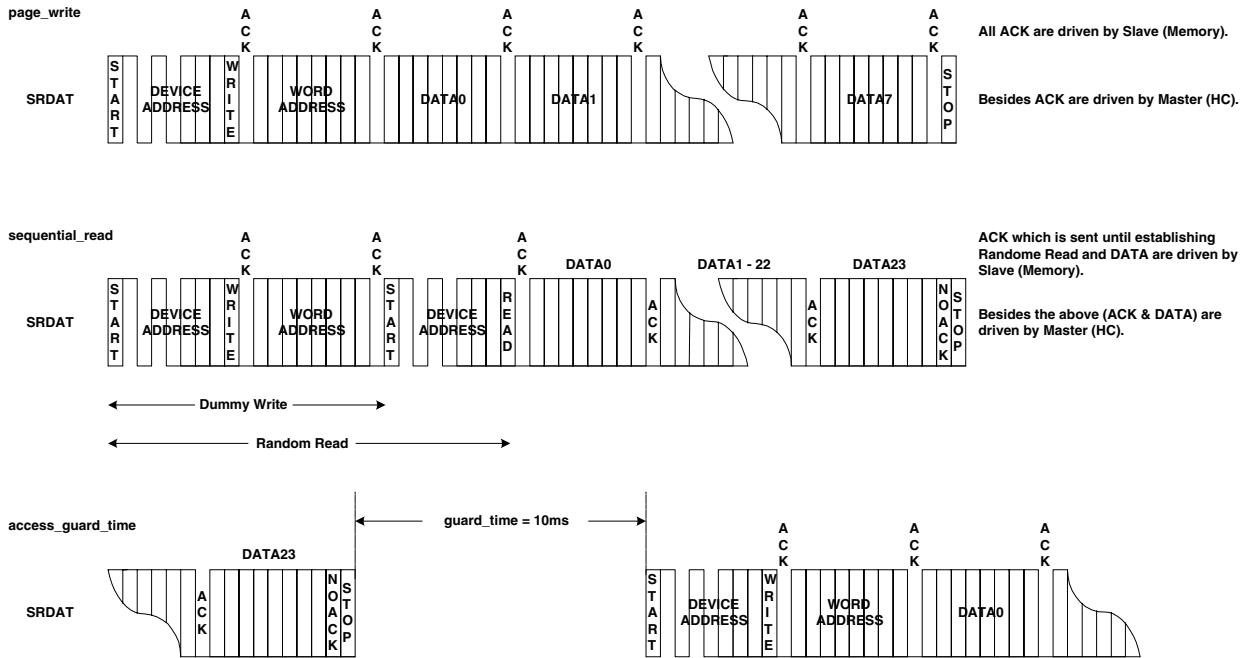
When external serial ROM is programmed for the first time, data for Page_0 to I2C_WND0 and I2C_WND1 shall be written first. When Page for Page Write field is written 00b and PWC is written a one at same time, the page_write command to Page_0 will be issued and 8 bytes data, which are set in I2C_WND0 and I2C_WND1, are written to external serial ROM. After page_write command is completed, the same thing for Page_1 followed by Page_2 shall be repeated.

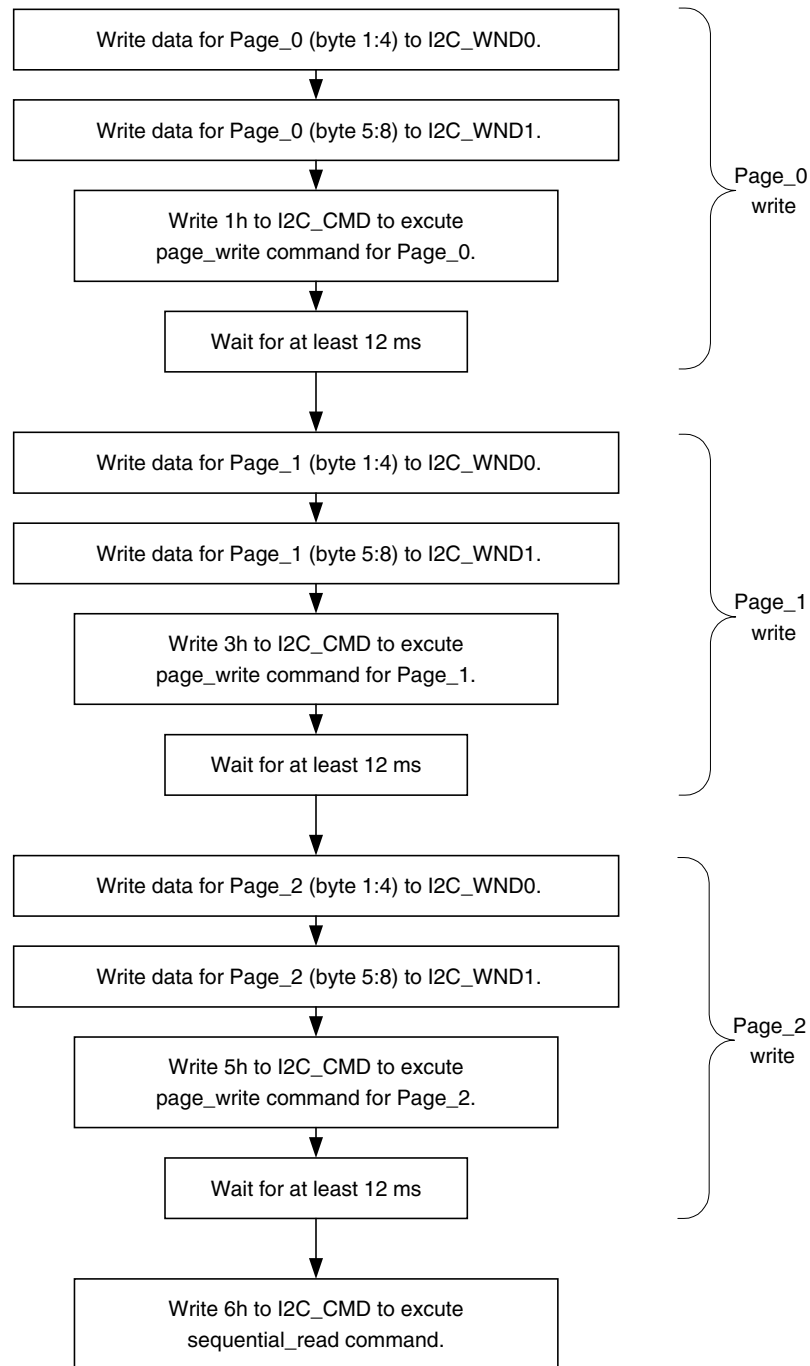**Figure 8-1. I2C_WND0/1 vs. Byte No.**

Timing chart for expected external serial ROM with I²C interface is as follows. This host controller issues "000b" for device address, and these three bits must correspond to hard-wired setting of serial ROM (Refer to **Figure 9-4. External Serial ROM Connection**).

Figure 8-2. I²C Timing Chart

It takes about 2 ms to complete page_write command. more than 12 ms shall be waited before starting next page_write or sequential_read command. On the other hands, It takes about 5 ms to complete sequential_read command. So, more than 15 ms shall be waited before starting next page_write or sequential_read command. And also more than 5 ms shall be waited before reading PCI configuration register after sequential_read command starts.

Figure 8-3. External Serial ROM Setting Flowchart
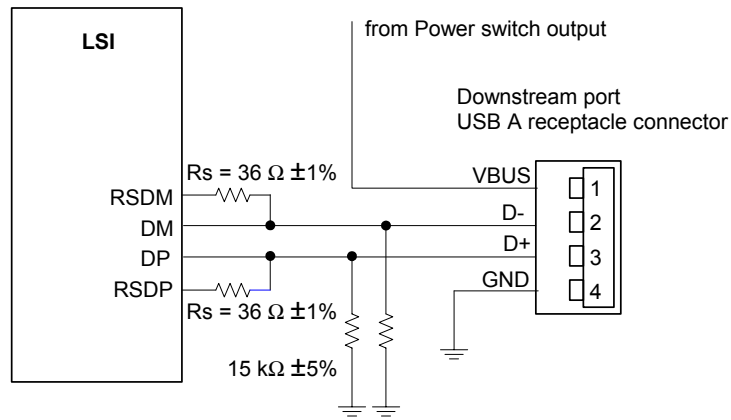
9.1 Handling Unused Pins

To realize less than 5 ports host controller implementation, appropriate value shall be set to Port No field in EXT1 register. And unused pins shall be connected as shown below.

Pin	Direction	Connection Method
DPx	I/O	Tied to "low".
DMx	I/O	Tied to "low".
RSDPx	O	No Connection (Open)
RSDMx	O	No Connection (Open)
OCIx	I	"H" clamp
PPONx	O	No Connection (Open)

9.2 USB Port Connection

★ **Figure 9-1. USB Downstream Port Connection**

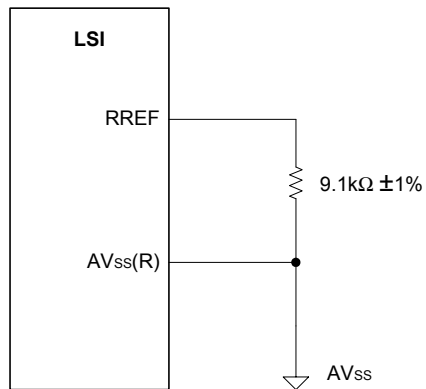Rs + Ron (Resistance for internal driver which is active) = 45 Ω ±10%
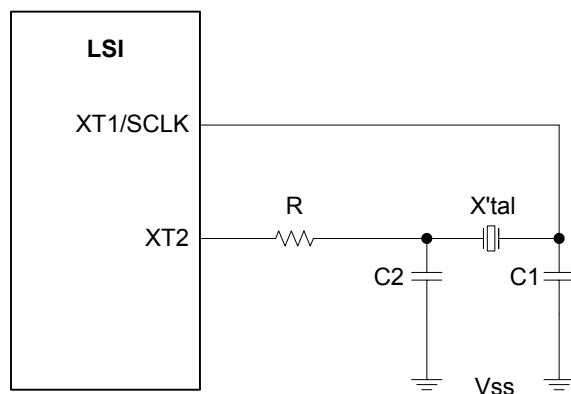
9.3 PLL Circuit Connection

★ **Figure 9-2. RREF Connection**

9.4 X'tal Connection

★ **Figure 9-3. X'tal Connection**

The following crystals are evaluated on our reference design board. Table 9-1 shows the external parameters.

Table 9-1. The External Parameters

Vender	X'tal	R	C1	C2
KDS [Note 1]	AT-49 30.000 MHz	100 Ω	12 pF	10 pF
NDK [Note 2]	AT-41 30.000 MHz	100 Ω	10 pF	10 pF
	AT-41CD2 30.000 MHz	100 Ω	10 pF	10 pF
	NX3225DA 30.000 MHz	100 Ω	10 pF	10 pF
	NX5032GA 30.000 MHz	100 Ω	10 pF	10 pF
	NX8045GB 30.000 MHz	100 Ω	10 pF	10 pF

Notes 1. DAISHINKU CORP.
2. NIHON DEMPA KOGYO CO., LTD.

In using these crystals, contact KDS or NDK to get the specification on external components to be used in conjunction with the crystal.
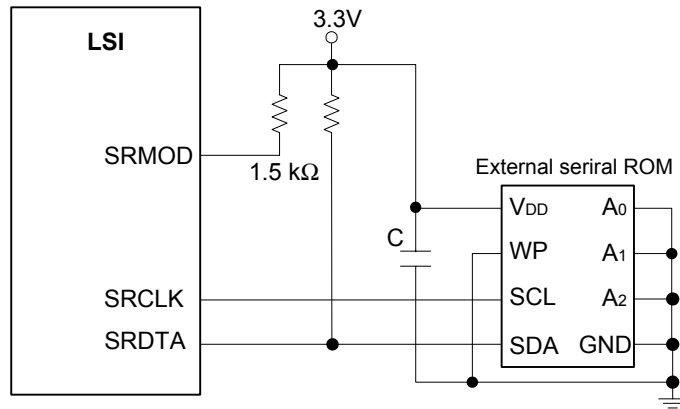
KDS's Home page: http://www.kdsj.co.jp
NDK's home page: http://www.ndk-j.co.jp

9.5 External Serial ROM Connection

★ **Figure 9-4. External Serial ROM Connection**

SRMOD/SRCLK/SRDTA can be opened, when serial ROM is not necessary on board.

CHAPTER 10 PRODUCT SPECIFICATIONS

10.1 Buffer List

- 3 V input buffer with pull down resistor
    - NTEST1, TEST, SRMOD, NANDTEST, SMC, AMC, TEB
- 3 V PCI I_{OL} = 9 mA 3-state output buffer
    - PPON (5:1), SRCLK
- 3 V I_{OL} = 9 mA bi-directional buffer
    - LEGC, SRDTA
- 3 V I_{OL} = 9 mA bi-directional buffer with enable (OR type)
    - OCI (5:1)
- 3 V oscillator interface
    - XT1/SCLK, XT2
- 5 V input buffer
    - VBBRST0, VCCRST0
- 5 V I_{OL} = 12 mA N-ch open drain buffer
    - SMI0, PME0, INTA0, INTB0, INTC0, SERR0
- 5 V PCI input buffer with enable (OR type)
    - PCLK, GNT0, IDSEL
- 5 V PCI I_{OL} = 12 mA 3-state output buffer
    - REQ0
- 5 V PCI I_{OL} = 9 mA bi-directional buffer with input enable (OR-type)
    - AD (31:0), CBE (3:0)0, PAR, FRAME0, IRDY0, TRDY0, STOP0, DEVSEL0, PERR0, CRUN0
- USB interface
    - DP (5:1), DM (5:1), RSDP (5:1), RSDM (5:1), RREF

Above, "5 V" refers to a 3 V buffer with 5 V tolerant circuit. Therefore, it is possible to have a 5 V connection for an external bus, but the output level will be only up to 3 V, which is the V_{DD} voltage. Similarly, "5 V PCI" above refers to a PCI buffer that has a 5 V tolerant circuit, which meets the 3 V PCI standard; it does not refer to a PCI buffer that meets the 5 V PCI standard.

10.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}, AV_{DD}, V_{DD_PCI}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}, AV_{DD}, V_{DD_PCI}	Indicates the voltage range for normal logic operations occur when $V_{SS} = 0$ V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the "Min." value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the "Max." value is applied, the input voltage is guaranteed as low level voltage.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

10.3 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}		−0.5 to +4.6	V
	AV_{DD}		−0.5 to +4.6	V
	V_{DD_PCI}		−0.5 to +6.0	V
Input voltage, 5 V buffer	V_I	$3.0\ V \le V_{DD} \le 3.6\ V$ $V_I < V_{DD} + 3.0\ V$	−0.5 to +6.6	V
Input voltage, 3.3 V buffer	V_I	$3.0\ V \le V_{DD} \le 3.6\ V$ $V_I < V_{DD} + 0.5\ V$	−0.5 to +4.6	V
Output voltage, 5 V buffer	V_O	$3.0\ V \le V_{DD} \le 3.6\ V$ $V_O < V_{DD} + 3.0\ V$	−0.5 to +6.6	V
Output voltage, 3.3 V buffer	V_O	$3.0\ V \le V_{DD} \le 3.6\ V$ $V_O < V_{DD} + 0.5\ V$	−0.5 to +4.6	V
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}		3.0	3.3	3.6	V
	AV_{DD}		3.0	3.3	3.6	V
	V_{DD_PCI}	In 3.3 V PCI	3.0	3.3	3.6	V
		In 5 V PCI	4.75	5.0	5.25	V
High-level input voltage	V_{IH}					
3.3 V high-level input voltage			2.0		V_{DD}	V
5.0 V high-level input voltage			2.0		5.5	V
Low-level input voltage	V_{IL}					
3.3 V low-level input voltage			0		0.8	V
5.0 V low-level input voltage			0		0.8	V

DC Characteristics (V_{DD} = 3.0 to 3.6 V, T_A = 0 to +70°C)

Control pin block

Parameter	Symbol	Condition	Min.	Max.	Unit
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or V_{SS}		±10	μA
Output short circuit current	I_{OS} **Note**			−250	mA
Low-level output current	I_{OL}				
3.3 V low-level output current		V_{OL} = 0.4 V	9.0		mA
3.3 V low-level output current		V_{OL} = 0.4 V	3.0		mA
5.0 V low-level output current		V_{OL} = 0.4 V	12.0		mA
5.0 V low-level output current		V_{OL} = 0.4 V	6.0		mA
High-level output current	I_{OH}				
3.3 V high-level output current		V_{OH} = 2.4 V	−9.0		mA
3.3 V high-level output current		V_{OH} = 2.4 V	−3.0		mA
5.0 V high-level output current		V_{OH} = 2.4 V	−2.0		mA
5.0 V high-level output current		V_{OH} = 2.4 V	−2.0		mA
Input leakage current	I_I				
3.3 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA
3.3 V buffer with 50 kΩ PD		$V_I = V_{DD}$		191	μA
5.0 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA

Note The output short circuit time is one second or less and is only for one pin on the LSI.

PCI interface block

Parameter	Symbol	Condition	Min.	Max.	Unit
High-level input voltage	V_{IH}		2.0	5.25	V
Low-level input voltage	V_{IL}		0	0.8	V
Low-level output current	I_{OL}	V_{OL} = 0.4 V	12.0		mA
High-level output current	I_{OH}	V_{OH} = 2.4 V	−2.0		mA
Input high leakage current	I_{IH}	V_{IN} = 2.7 V		70	μA
Input low leakage current	I_{IL}	V_{IN} = 0.5 V		−70	μA
PME0 leakage current	I_{OFF}	V_O < 3.6 V V_{CC} off or floating		1	μA

USB interface block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Serial resistor between DP (DM) and RSDP (RSDM)	R_S		35.64	36.36	Ω
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	$\left|(D+) - (D-)\right|$	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		−50	+500	mV
High-speed differential input signaling level	See **Figure 10-4**.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		−10	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		−10	+10	mV
Chirp J level (differential signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (differential signal)	V_{CHIRPK}		−900	−500	mV

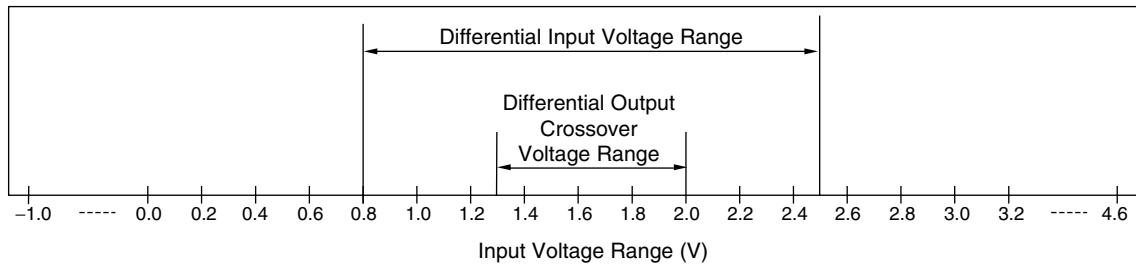**Figure 10-1. Differential Input Sensitivity Range for Low-/Full-speed**

Figure 10-2. Full-speed Buffer V$_{OH}$/I$_{OH}$ Characteristics for High-speed Capable Transceiver
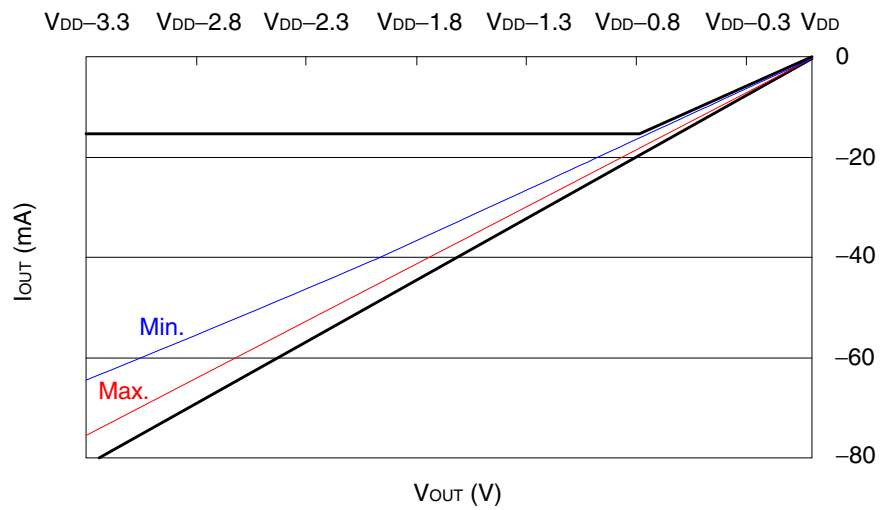

Figure 10-3. Full-speed Buffer V$_{OL}$/I$_{OL}$ Characteristics for High-speed Capable Transceiver
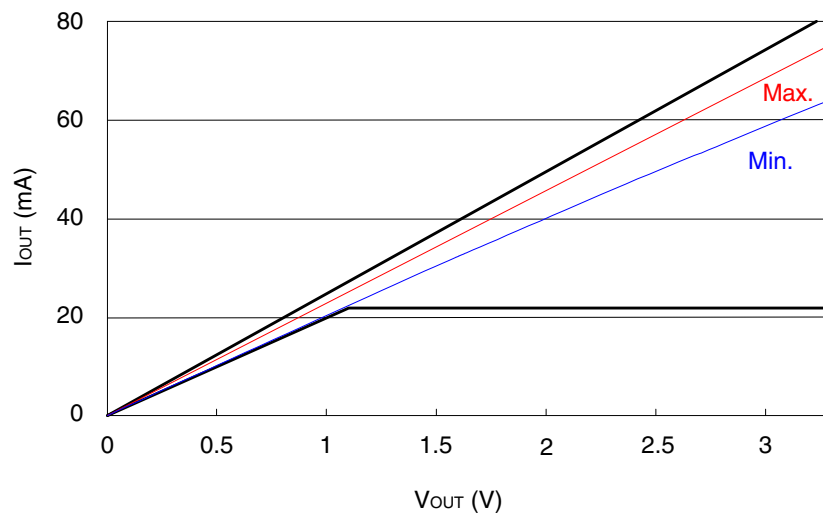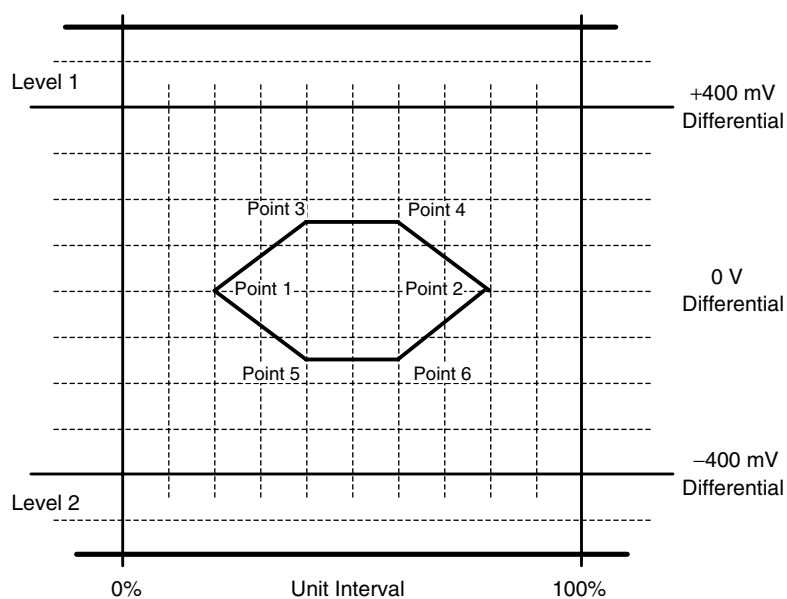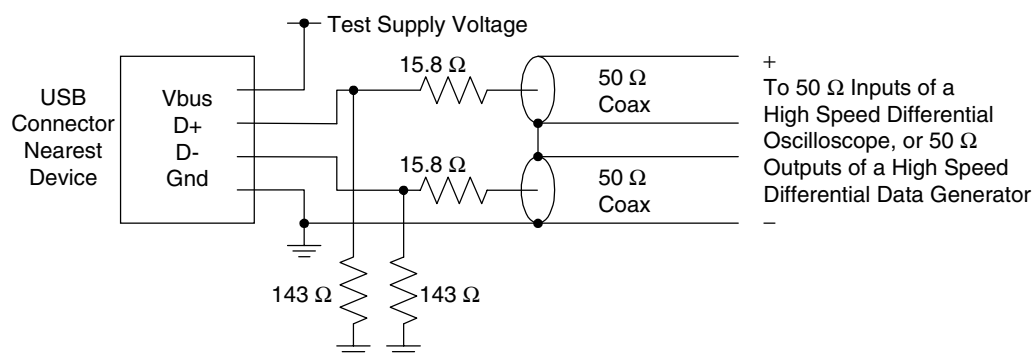
Figure 10-4. Receiver Sensitivity for Transceiver at DP/DM

Figure 10-5. Receiver Measurement Fixtures

Pin capacitance

Parameter	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_I	$V_{DD} = 0$ V, $T_A = 25$ °C	6	8	pF
Output capacitance	C_O	$f_C = 1$ MHz	10	12	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V	10	12	pF
PCI input pin capacitance	C_{in}			8	pF
PCI clock input pin capacitance	C_{clk}		6	8	pF
PCI IDSEL input pin capacitance	C_{IDSEL}			8	pF

Power consumption

Parameter	Symbol	Condition	Typ. (30 MHz X'tal)	Typ. (48 MHz OSC)	Unit
Power Consumption	$P_{WD0\text{-}0}$	Device state = D0, All the ports does not connect to any function, and each OHCI controller is under UsbSuspend and EHCI controller is stopped. [Note1]	31.4	10.4	mA
	$P_{WD0\text{-}1}$	The power consumption under the state without suspend. Device state = D0, The number of active ports is 1. [Note2]			
		Full- or low-speed device(s) is (are) on the port.	43.6	22.6	mA
		High-speed device(s) is (are) on the port.	156.6	156.8	mA
	$P_{WD0\text{-}2}$	The power consumption under the state without suspend. Device state = D0, The number of active ports is 2. [Note2]			
		Full- or low-speed device(s) is (are) on the port.	53.1	31.9	mA
		High-speed device(s) is (are) on the port.	204.6	204.2	mA
	$P_{WD0\text{-}3}$	The power consumption under the state without suspend. Device state = D0, The number of active ports is 3. [Note2]			
		Full- or low-speed device(s) is (are) on the port.	55.3	34.2	mA
		High-speed device(s) is (are) on the port.	253.8	255.5	mA
	$P_{WD0\text{-}4}$	The power consumption under the state without suspend. Device state = D0, The number of active ports is 4. [Note2]			
		Full- or low-speed device(s) is (are) on the port.	57.4	36.7	mA
		High-speed device(s) is (are) on the port.	301.6	300.1	mA
	$P_{WD0\text{-}5}$	The power consumption under the state without suspend. Device state = D0, The number of active ports is 5. [Note2]			
		Full- or low-speed device(s) is (are) on the port.	59.8	38.8	mA
		High-speed device(s) is (are) on the port.	349.1	345.2	mA
	P_{WD0_C}	The power consumption under suspend state during PCI clock is stopped by CRUN0. Device state = D0.	30.5	10.4	mA
	P_{WD1}	Device state = D1, Analog PLL output is stopped. [Note 3]	7.7	10.4	mA
	P_{WD2}	Device state = D2, Analog PLL output is stopped. [Note 3]	7.7	10.4	mA
	P_{WD3H}	Device state = $D3_{hot}$, VCCRST0 = High, Analog PLL output is stopped. [Note 3]	7.7	10.4	mA
	P_{WD3C}	Device state = $D3_{cold}$, VCCRST0 = Low. [Note 4]	0.03	3.81	mA

Notes 1. When any device is not connected to all the ports of HC, the power consumption for HC does not depend on the number of active ports.

2. The number of active ports is set by the value of Port No Field in PCI configuration space EXT register.

3. This is the case when PCI bus state is B0.

4. This is the case when PCI bus state is B3.

Remark These are estimated value on Windows™ XP environment.

System clock ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_{CLK}	X'tal	−500 ppm	30	+500 ppm	MHz
		Oscillator block	−500 ppm	48	+500 ppm	MHz
Clock duty cycle	t_{DUTY}		40	50	60	%

Remarks 1. Recommended accuracy of clock frequency is $\pm$ 100 ppm.

2. Required accuracy of X'tal or oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

AC Characteristics (V_{DD} = 3.0 to 3.6 V, T_A = 0 to +70°C)

PCI interface block

Parameter	Symbol	Condition	Min.	Max.	Unit
PCI clock cycle time	t_{cyc}		30		ns
PCI clock pulse, high-level width	t_{high}		11		ns
PCI clock pulse, low-level width	t_{low}		11		ns
PCI clock, rise slew rate	S_{cr}	$0.2V_{DD}$ to $0.6V_{DD}$	1	4	V/ns
PCI clock, fall slew rate	S_{cf}	$0.2V_{DD}$ to $0.6V_{DD}$	1	4	V/ns
PCI reset active time (vs. power supply stability)	t_{rst}		1		ms
PCI reset active time (vs. CLK start)	$t_{rst-clk}$		100		μs
Output float delay time (vs. RST0$\downarrow$)	$t_{rst-off}$			40	ns
PCI reset rise slew rate	S_{rr}		50		mV/ns
PCI bus signal output time (vs. PCLK$\uparrow$)	t_{val}		2	11	ns
PCI point-to-point signal output time (vs. PCLK$\uparrow$)	t_{val} (ptp)	REQ0	2	12	ns
Output delay time (vs. PCLK$\uparrow$)	t_{on}		2		ns
Output float delay time (vs. PCLK$\uparrow$)	t_{off}			28	ns
Input setup time (vs. PCLK$\uparrow$)	t_{su}		7		ns
Point-to-point input setup time (vs. PCLK$\uparrow$)	t_{su} (ptp)	GNT0	10		ns
Input hold time	t_h		0		ns

USB interface block

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Parameter	Symbol	Conditions	Min.	Max.	Unit
Low-speed Source Electrical Characteristics					
Rise time (10 to 90%)	t_{LR}	C_L = 200 to 600 pF, R_S = 36 Ω	75	300	ns
Fall time (90 to 10%)	t_{LF}	C_L = 200 to 600 pF, R_S = 36 Ω	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF})	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps

Source jitter total (including frequency tolerance):
    To next transition
    For paired transitions
	t_{DDJ1}
	t_{DDJ2}
			−25
			−14
				+25
				+14
					ns
					ns

Source jitter for differential transition to SE0 transition	t_{LDEOP}		−40	+100	ns

Receiver jitter:
    To next transition
    For paired transitions
	t_{UJR1}
	t_{UJR2}
			−152
			−200
				+152
				+200
					ns
					ns

Source SE0 interval of EOP	t_{LEOPT}		1.25	1.50	μs
Receiver SE0 interval of EOP	t_{LEOPR}		670		ns
Width of SE0 interval during differential transition	t_{FST}			210	ns
Full-speed Source Electrical Characteristics					
Rise time (10 to 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90 to 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns

Source jitter total (including frequency tolerance):
    To next transition
    For paired transitions
	t_{DJ1}
	t_{DJ2}
			−3.5
			−4.0
				+3.5
				+4.0
					ns
					ns

Source jitter for differential transition to SE0 transition	t_{FDEOP}		−2	+5	ns

Receiver jitter:
    To next transition
    For paired transitions
	t_{JR1}
	t_{JR2}
			−18.5
			−9
				+18.5
				+9
					ns
					ns

Source SE0 interval of EOP	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns

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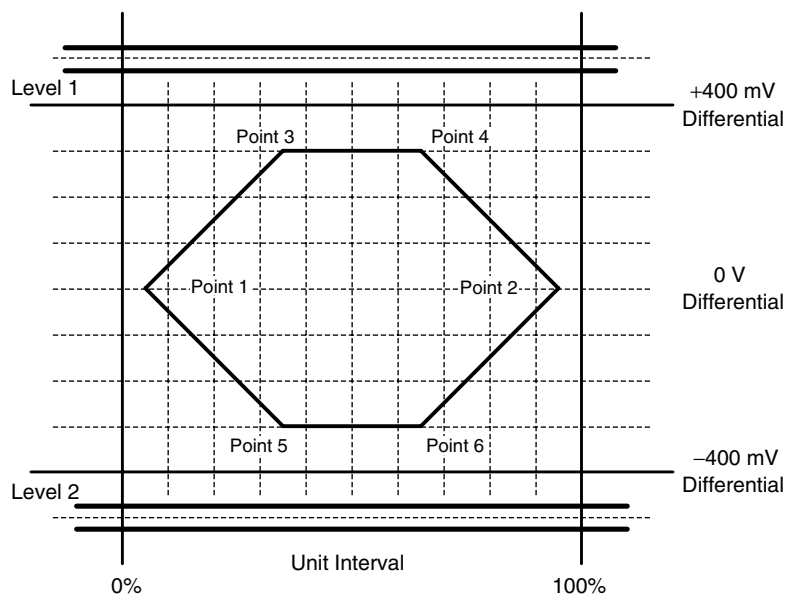| Parameter	Symbol	Conditions	Min.	Max.	Unit
High-speed Source Electrical Characteristics					
Rise time (10 to 90%)	t_{HSR}		500		ps
Fall time (90 to 10%)	t_{HSF}		500		ps
Driver waveform	See **Figure 10-6**.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See **Figure 10-6**.				
Receiver jitter tolerance	See **Figure 10-4**.				
Hub Event Timings					
Time to detect a downstream facing port connect event	t_{DCNN}		2.5	2000	μs
Time to detect a disconnect event at a hub's downstream facing port	t_{DDIS}		2.0	2.5	μs
Duration of driving resume to a downstream port	t_{DRSMDN}	Nominal	20		ms
Time from detecting downstream resume to rebroadcast	t_{URSM}			1.0	ms
Inter-packet delay for packets traveling in same direction for high-speed	$t_{HSIPDSD}$		88		Bit times
Inter-packet delay for packets traveling in opposite direction for high-speed	$t_{HSIPDOD}$		8		Bit times
Inter-packet delay for root hub response for high-speed	$t_{HSRSPIPD1}$			192	Bit times
Time for which a Chirp J or Chirp K must be continuously detected during reset handshake	t_{FILT}		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K	t_{WTDCH}			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream during reset	t_{DCHBIT}		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	t_{DCHSE0}		100	500	μs

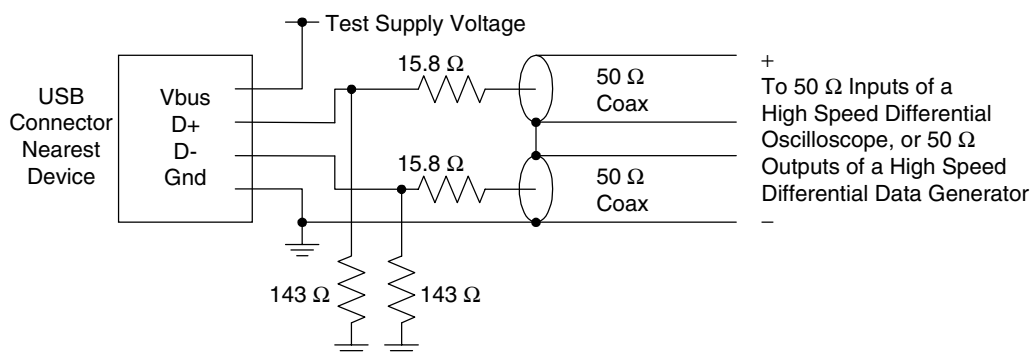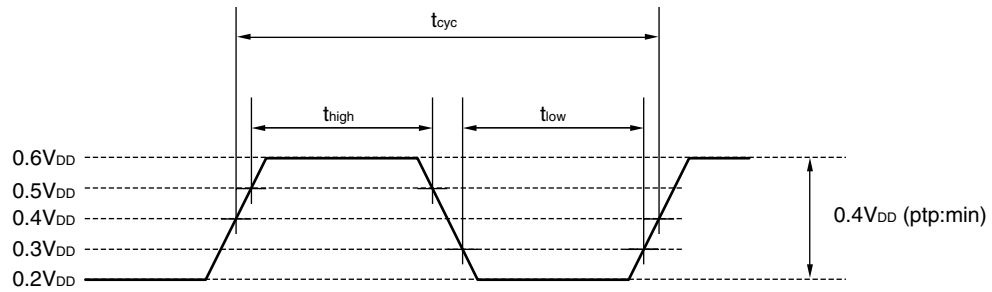**Figure 10-6. Transmit Waveform for Transceiver at DP/DM**

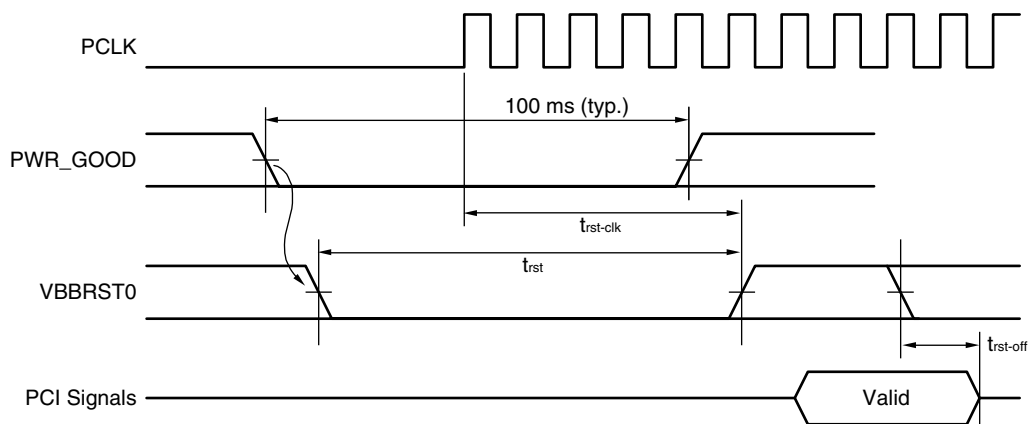**Figure 10-7. Transmitter Measurement Fixtures**
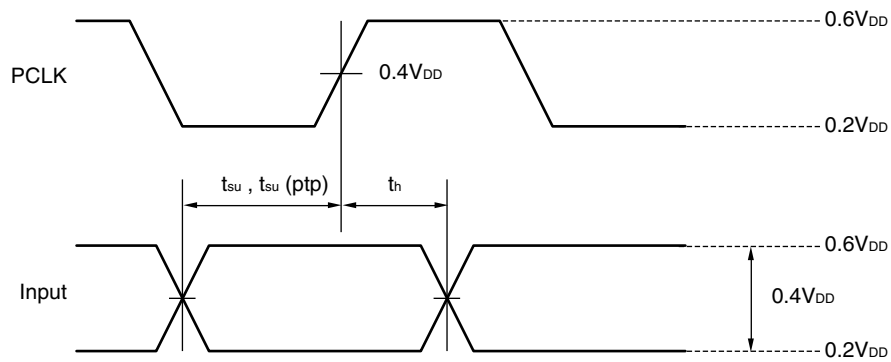
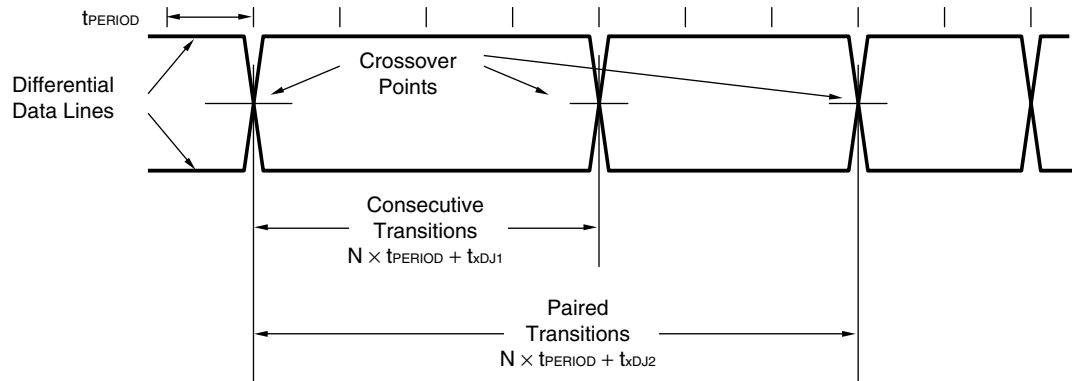## 10.4 Timing Diagram

PCI clock

PCI reset

PCI output timing measurement condition
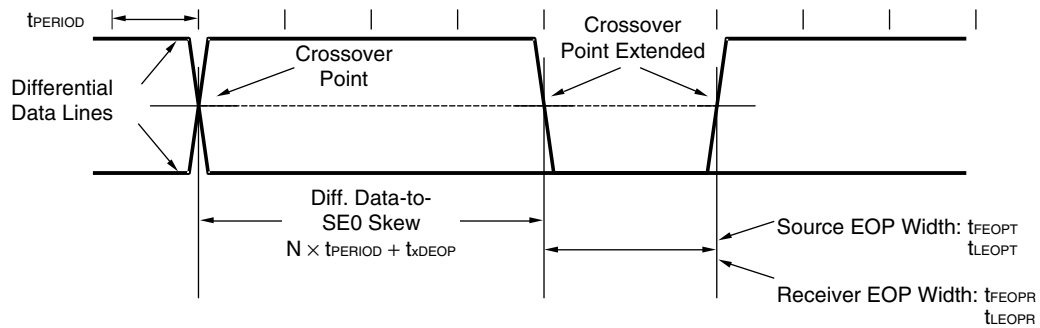
PCLK

0.6V$_{DD}$

0.4V$_{DD}$

0.2V$_{DD}$

t$_{val}$, t$_{val}$ (ptp)

Output delay

0.615V$_{DD}$ (for falling edge)

0.285V$_{DD}$ (for falling edge)

Output

t$_{on}$

t$_{off}$

PCI input timing measurement condition

PCLK

0.6V$_{DD}$

0.4V$_{DD}$

0.2V$_{DD}$

t$_{su}$, t$_{su}$ (ptp)

t$_{h}$

Input

0.6V$_{DD}$

0.4V$_{DD}$

0.2V$_{DD}$

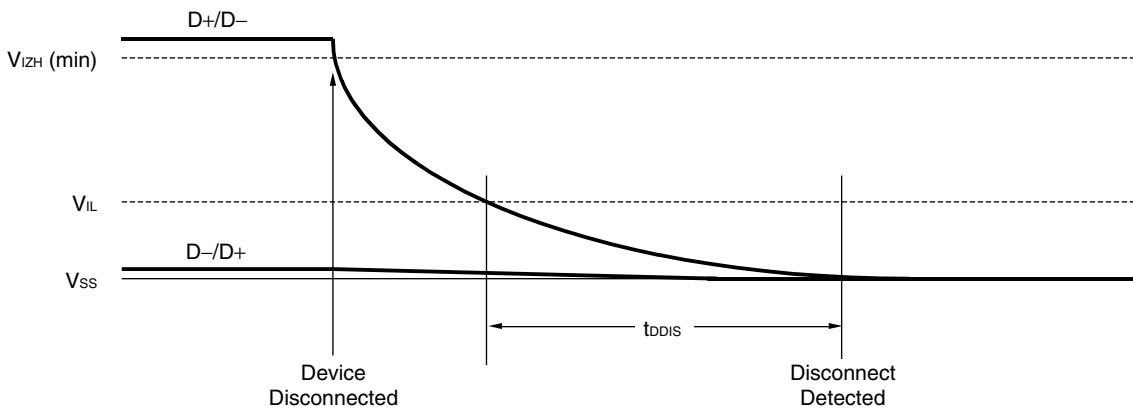**USB differential data jitter for full-speed**

USB differential-to-EOP transition skew and EOP width for low-/full-speed
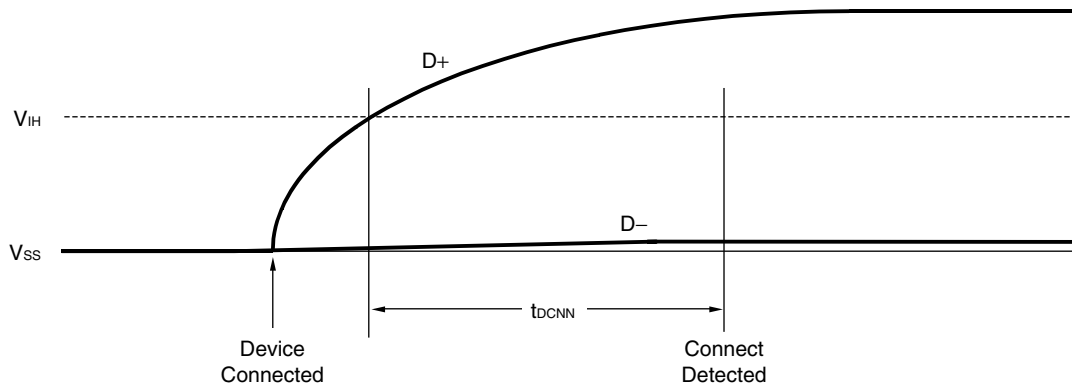

USB receiver jitter tolerance for low-/full-speed

Low-/full-speed disconnect detection

Full-/high-speed device connect detection

Low-speed device connect detection