CTPci Hardware Guide

Rev.1.8a
February 21st, 2006 to April 2010 © Rodolphe Czuba

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Summary

Conventions

The MPC860 mode is selected on PCI9054 to connect with 68060. Thus the IBM PowerPC convention is used :
32-bits data is written D[0:31] with D0 for MSB and D31 for LSB.
Same for address bits and all control bits like TSIZ[0:1].
For information :
- PCI9054 Data D[0:31] bits are connected respectively to MC68060 D[31:0] data bits.
- PCI9054 Address A[0:31] bits are connected respectively to MC68060 A[31:0] address bits.
- Same for some control signals (PCI9054 TSIZ[0:1] with 060 SIZ[1:0] by example).

PCI 9054 Data Assignment :

Data Width	PCI 9054 & 060 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	Lword

Falcon CT60/63 CTPCI 32-Bit MAP

Falcon				
$00000000	$00DFFFFF	14 MB	ST-RAM	CACHE - NO BURST
$00E00000	$00EFFFFF	1 MB	**CT60/63 FLASH**	CACHE - NO BURST
$00F00000	$00F0FFFF	64 KB	IDE Port	NO CACHE - NO BURST
$00F10000	$00F9FFFF	576 KB	F030 BUS Port	NO CACHE - NO BURST
$00FA0000	$00FBFFFF	128 KB	CARTRIDGE Port	NO CACHE - NO BURST
$00FC0000	$00FEFFFF	192 KB	*Unused*	NO CACHE - NO BURST
$00FF0000	$00FFFFFF	64 KB	I/O	NO CACHE - NO BURST
SDRAM – Cache & Burst				
$01000000	$04FFFFFF	64 MB	SDRAM (TT-RAM)	
$01000000	$08FFFFFF	128 MB	SDRAM (TT-RAM)	
$01000000	$10FFFFFF	256 MB	SDRAM (TT-RAM)	
$01000000	$20FFFFFF	512 MB	SDRAM (TT-RAM)	
CT60 SLOT - Cache & Burst				
$21000000	$2FFFFFFF	240 MB	*Reserved*	
$30000000	$3FFFFFFF	256 MB	SUPERVIDEL DDR SDRAM	
$40000000	**$5FFFFFFF**	**512 MB**	**CTPCI : PCI MEM Space**	**NO CACHE**
$60000000	$7FFFFFFF	512 MB	*Reserved*	
CT60 SLOT - No Cache/Burst				
$80000000	$8000003F	256 B	EtherNAT	INT. Vectors $C4 & $C5
$80000040	$8FFFFFFF	255 MB	*Reserved*	
$90000000	$BFFFFFFF	768 MB	*Reserved*	
$C0000000	**$DFFFFFFF**	**512 MB**	**CTPCI : PCI I/O Space**	
$E0000000	**$E7FFFFFF**	**128 MB**	**CTPCI : CPLD Registers**	
$E8000000	**$EFFFFFFF**	**128 MB**	**CTPCI : PLX Registers**	
I/O – No Cache/Burst				
$F0000000	$FBFFFFFF	192 MB	CT60/63 Registers	
$FCF00000	**$FCF0FFFF**	**64KB**	**Second IDE Port**	
$FD000000	$FEFFFFFF	32 MB	*Reserved*	
$FF000000	$FFFFFFFF	16 MB	FALCON 24-Bit SHADOW	

PLX 9054 BRIDGE OVERVIEW

The PCI 9054, a 32-bit 33-MHz PCI Bus Master I/O Accelerator, is the most advanced general-purpose bus Master device available. It offers a robust PCI Specification v2.2 implementation enabling Burst transfers up to 132 MB/second. The PCI 9054 incorporates the industry leading PLX Data Pipe Architecture™ technology, including DMA engines, programmable PCI Initiator and Target Data-Transfer modes, and PCI messaging functions
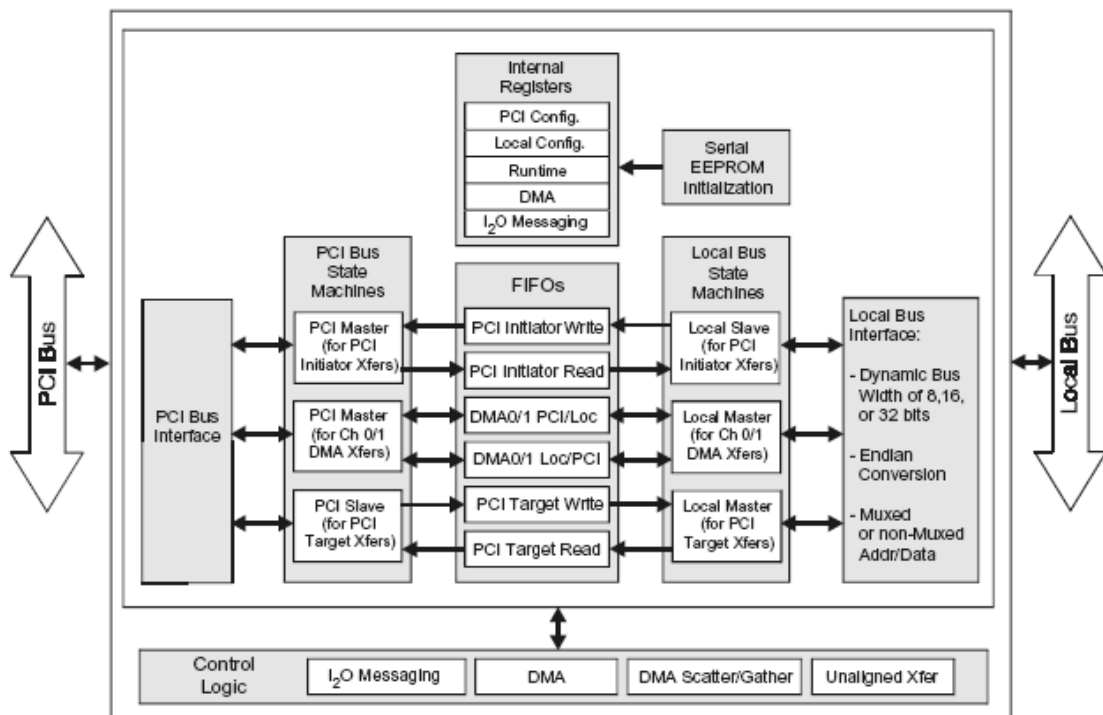

Figure 1-2. PCI 9054 Internal Block Diagram

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Register Compatibility
All registers implemented in the PCI 9080 (Milan Bridge) are implemented in the PCI 9054. The PCI 9054 includes many new bit definitions and several new registers.

EEPROM is not present
The Local processor programs the PCI 9054 registers, then sets the Local Init Status bit (LMISC[2]=done).
Note: Some systems may hang if PCI Target reads and writes take too long (during initialization, the PCI Host also performs PCI Target accesses). The value of the PCI Target Retry Delay Clocks (LBRD0[31:28]) may resolve this.

Features of bridge on the CTPCI

• PCI Specification version 2.2 (v2.2) compliant 32-bit, 33-MHz Bus Master Interface Controller with PCI Power Management features for adapters and embedded systems
• PCI v2.2 Vital Product Data (VPD) configuration support
• PCI ↔ Local Data transfers up to 132 MB/s
• 3.3V, 5V tolerant PCI and Local signaling supports Universal PCI Adapter designs, 3.3V core, lowpower CMOS in 176-pin PQFP
• Industrial Temp Range operation
• Subsystem ID and Subsystem Vendor ID.
        Contains Subsystem ID and Subsystem Vendor ID in the PCI Configuration Register Space in addition to
        System and Vendor IDs. The PCI 9054 also contains a permanent Vendor ID (10B5h) and Device ID (9054h).
• PCI Dual Address Cycle (DAC) support
• PCI Hot Plug and CompactPCI Hot Swap compliant
• I2O™ v1.5-Ready Messaging Unit
• Two independent DMA channels for Local Bus memory to and from PCI Host Bus Data transfers
        Can transfer data on any byte-boundary combination of the PCI and Local Address spaces.
• Programmable Burst Management
• Programmable Interrupt Generator
        Can assert PCI and Local interrupts from external and internal sources.
• Six programmable FIFOs for zero wait state burst operation

FIFO	Length
PCI Initiator Read	16 Lwords
PCI Initiator Write	32 Lwords
PCI Target Read	16 Lwords
PCI Target Write	32 Lwords
DMA Read	32 Lwords
DMA Write	32 Lwords

• Programmable Local Bus runs up to 50 MHz and supports non-multiplexed 32-bit address/data and slave accesses of 8-, 16-, or 32-bit Local Bus devices.

The PCI 9054 communicates using four possible Data-Transfer modes:
- • Configuration Register Access
- • PCI Initiator Operation
- • PCI Target Operation
- • DMA Operation

• Local Bus runs asynchronously to the PCI Bus

The clock on CT bus is from 66 to 105 MHz and the Bridge local clock is half the CT bus clock → 33 to 52.5 MHz. The PCI clock is 33 MHz.

• Three PCI-to-Local Address spaces

The PCI 9054 supports three PCI-to-Local Address spaces when the PCI 9054 is in PCI Target or PCI Slave mode. These spaces (Space 0, Space 1, and Expansion ROM spaces) allow any PCI Bus Master to access the Local Memory spaces with programmable wait states, bus width, burst capabilities, and so forth.

On CTPCI-CT60/63 the following space are attributed :

Space #0 = SDRAM – 32-bits on CT with NO BURST.

Space #1 = ST-RAM – 32-bits on CT with NO BURST.

Space ROM = FLASH – 32-bits on CT with NO BURST.

• Eight 32-bit Mailbox

May be accessed from the PCI or Local Bus.

• Two 32-bit Doorbell registers

One asserts interrupts from the PCI Bus to the Local Bus. The other asserts interrupts from the Local Bus to the PCI Bus.

• Performs Big Endian ↔Little Endian conversion

Supports dynamic switching between Big Endian (Address Invariance) and Little Endian (Data Invariance) operations for PCI Target, PCI Initiator, DMA, and internal register accesses on the Local Bus.

The PCI 9054 supports on-the-fly Endian conversion for Space 0, Space 1, and Expansion ROM space.

The Local Bus is BIG ENDIAN programmed with the BIGEND# input pin.

Note: The PCI Bus is always Little Endian.

• Programmable prefetch counter

The PCI 9054 can be programmed to prefetch data during PCI Target and PCI Initiator prefetches (known or unknown size). To perform burst reads, prefetching must be enabled. The prefetch size can be programmed to match the Master burst length, or can be used as Read Ahead mode data. The PCI 9054 reads single data (8, 16, or 32 bit) if the Master initiates a single cycle; otherwise, the PCI 9054 prefetches the programmed size.

• PCI-to-Local Delayed Read mode

Supports Read Ahead mode, where prefetched data can be read from the PCI 9054 internal PCI Target Read FIFO instead of from the Local Bus. The address must be subsequent to the previous address and 32-bit aligned (next address = current address + 4). This feature allows for increased bandwidth and reduced data latency.

• Posted Memory Writes.

Supports the Posted Memory Writes (PMW) for maximum performance and to avoid potential deadlock situations.

• Keep Bus Mode

The PCI 9054 can be programmed to keep the PCI Bus by generating wait state(s) if the PCI Target Write FIFO becomes full.

The PCI 9054 can also be programmed to keep the Local Bus (LHOLD asserted) if the PCI Target Write FIFO becomes empty or the PCI Target Read FIFO becomes full.

The Local Bus is dropped in either case when the Local Bus Latency Timer is enabled and expires.

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PLX 9054 and PLX 9080 (Milan) Comparison

Feature	PCI 9054	PCI 9080
Package Size/Type	176 PQFP, 225 PBGA	208 PQFP
Number of DMA Channels	2	2
Local Address Spaces	3	3
PCI Initiator Mode	Yes	Yes
Mailbox Registers	Eight 32-bit	Eight 32-bit
Doorbell Registers	Two 32-bit	Two 32-bit
Number of FIFOs	6	8
FIFO Depth—PCI Target Write and PCI Initiator Write	32 Lwords (128 bytes)	32 Lwords (128 bytes)
FIFO Depth—PCI Target Read and PCI Initiator Read	16 Lwords (64 bytes)	16 Lwords (64 bytes)
FIFO Depth—DMA Channel 0	32 Lwords (128 bytes) Single bidirectional Read/Write FIFO	32 Lwords (128 bytes) Read and Write FIFOs
FIFO Depth—DMA Channel 1	16 Lwords (64 bytes) Single bidirectional Read/Write FIFO	16 Lwords (64 bytes) Read and Write FIFOs
LLOCKo# Pin for Lock Cycles	Yes	Yes
WAIT# Pin for Wait State Generation	Yes	Yes
BPCLKo Pin; Buffered PCI Clock	No	Yes
DREQ0# and DACK0# Pins for Demand Mode DMA Support	Yes (One channel only)	Yes
Register Addresses	Identical to the PCI 9080 except the PCI 9054 contains additional registers related to added functionality	—
Big Endian ↔ Little Endian Conversion	Yes	Yes
PCI Specification v2.1 Deferred Reads	Yes	Yes
PCI Specification v2.2 PCI Power Management, PCI Hot Plug Compliant, CompactPCI Hot Swap Compliant	Yes	No
PCI v2.2 VPD Support	Yes	No
Programmable Prefetch Counter	Yes	Yes
Memory Write and Invalidate Cycle	Yes	Yes
Additional Device and Vendor ID Registers	Yes	Yes
I_2O Messaging Unit	Yes	Yes
Core and Local Bus Vcc	3.3V	5V
PCI Bus Vcc	3.3V	3.3/5V
3.3V PCI Bus and Local Bus Signaling	Yes	Yes (if PCI Vcc is 3.3V)
5V Tolerant PCI Bus and Local Bus	Yes	Yes (if PCI Vcc is 5V)
Serial EEPROM Support	2K bit, 4K bit devices	1K bit, 2K bit devices
Serial EEPROM Read Control	Reads allowed via Vital Product Data Function (refer to Section 10)	Reads allowed via Serial EEPROM Control Register (CNTRL)

LOCAL PINS

LOCAL BUS pins (M mode) used on CTPCI

CCS#	Configuration Register Select	IN	Internal PCI 9054 registers are selected when CCS# is asserted low.
LCLK	Local Clock	IN	Local clock input.
LINT#	Local Interrupt	BI	As an input to the PCI 9054, when asserted low, causes a PCI interrupt. Not used on CTPCI. As an output, a synchronous level output that remains asserted as long as an interrupt condition exists. If edge level interrupt is required, disabling and then enabling Local interrupts through INTCSR creates an edge if an interrupt condition still exists or a new interrupt condition occurs.
BB#	Bus Busy	BI	As an input, monitors this signal to determine whether the external Master has ended a Bus cycle. As an output, asserts this signal after an external arbiter has granted ownership of the Local Bus and BB# is inactive from another Master.
BDIP#	Burst Data in progress	BI	As an input, driven by the Bus Master during a Burst transaction. The Master de-asserts before the last Data phase on the bus. As an output, driven by the PCI 9054 during the Data phase of a Burst transaction. The PCI 9054 de-asserts before the last Burst Data phase on the bus.
BG#	Bus Grant	I	Asserted by the Local Bus arbiter in response to BR#. Indicates the requesting Master is next.
BI#	Burst Inhibit	I	Whenever BI# is asserted, indicates that the Target device does not support Burst transactions.
BR#	Bus Request	OUT	Asserted by the Master to request use of the Local Bus. The Local Bus arbiter asserts BG# when the Master is next in line for bus ownership.
BURST#	Burst	BI	As an input, driven by the Master along with address and data indicating a Burst transfer is in progress. As an output, driven by the PCI 9054 along with address and data indicating a Burst transfer is in progress.
LA[0:31]	Address Bus	BI	Carries the 32 bits of the physical Address Bus. LA0 is most significant bit of bus address.
LD[0:31]	Data Bus	BI	All Master accesses to the PCI 9054 are 32 bits only. LD0 is most significant bit of bus address.
RD/WR#	Read/Write	BI	Asserted high for reads and low for writes.
RETRY#	Retry	OUT	Driven by the PCI 9054 when it is a Slave to indicate a Local Master must back off and restart the cycle. In Deferred Read mode, indicates a Local Master should return for the requested data.
TA#	Transfer Acknowledge	BI	As an input, when a Local Bus access is made to the PCI 9054, indicates a Write Data transfer can complete or that Read data on the bus is valid. As an output, when the PCI 9054 is a Bus Master, indicates a Write Data transfer is complete or that Read data on the bus is valid.
TEA#	Transfer Error Ack	BI	Driven by the Target device, indicating an error condition occurred during a Bus cycle.
TS#	Address Strobe	BI	Indicates the valid address and start of a new Bus access. Asserted for the first clock of a Bus access.
TSIZ[0:1]	Transfer Size	BI	Driven by the current Master along with the address, indicating the data-transfer size. TSIZ0 is most significant bit of bus address. Refer to Section 3.4.3.5 for further information.
MDREQ#/	IDMA Data Transfer Request	OUT	Multiplexed input or output pin : **MDREQ#**: IDMA M mode Data transfer request start. Always asserted, indicating Data transfer should start. De-asserted only when the PCI Initiator FIFO becomes full. Programmable through a Configuration register.
DMPAF/	**PCI Initiator Programmable Almost Full**	**OUT**	**DMPAF**: PCI Initiator Write FIFO Almost Full status output. Programmable through a Configuration register. Connected to CPLD as INT source.
EOT#	End of Transfer for Current DMA Channel	IN	**EOT#:** Terminates the current DMA transfer. *Note: EOT# serves as a general purpose EOT. Before asserting EOT#, user should be aware of DMA channel activity.*

LOCAL BUS pins (M mode) NOT used on CTPCI

BIGEND#	Big Endian Select	IN	Multiplexed input or output pin : Can be asserted during the Local Bus Address phase of a PCI Initiator transfer or Configuration register access to specify use of Big Endian Byte ordering. Big Endian Byte order for PCI Initiator transfers or Configuration register accesses is also programmable through the Configuration registers.
WAIT#	WAIT Input/Output Select	BI	PCI 9054 issues WAIT# when it is a Master on the Local Bus and has internal wait states setup. As a Slave, the PCI 9054 accepts WAIT# as an input from the Bus Master.
DP[0:3]	Data Parity	BI	Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for writes or reads to the PCI 9054. Parity is asserted for reads from or writes by the PCI 9054. DP0 is the most significant bit of the Bus address.
LRESETo#	Local Bus Reset Ou	OUT	Asserted when the PCI 9054 chip is reset. Can be used to drive RESET# input of a Local processor.

SERIAL EEPROM pins - NOT USED ON CTPCI

EECS	Serial EEPROM Chip Select	IN	Serial EEPROM Chip Select.
EEDI/ EEDO	Serial EEPROM Data IN/ Serial EEPROM Data OUT	BI	Multiplexed Write/Read data to a serial EEPROM pin. These pins have internal pull-ups.
EESK	Serial Data Clock	IN	Serial EEPROM clock pin.

HOT SWAP pins - NOT USED ON CTPCI

ENUM#	Enumeration	OUT	Interrupt output asserted when an adapter using PCI 9054 has been freshly inserted or is ready to be removed from a PCI slot.
LEDon/ LEDin	LEDon/LEDin	OUT/ IN	As an output, acts as the Hot Swap board indicator LED. As an input, monitors the CompactPCI board latch status.

CONFIGURATION pins

MODE[1:0]	Bus Mode	IN	Selects the PCI 9054 bus operation mode: Mode [1:0] = [1,1] → MODE M for CTPCI These pins have internal pull-ups.
TEST	Test Pin	IN	Pulled high for test and low for normal operation. <u>When pulled high:</u> All outputs except USERo/DREQ0#/LLOCKo# and LEDon/LEDin are placed in tri-state. USERo/DREQ0#/LLOCKo# provides NANDTREE output. The TEST pin has an internal pull-down.

The following pins have internal pull-ups :

BI#, BIGEND#/WAIT#, BURST#, CCS#, DP[3:0]#,
LA[0:1], LA[3:31], LAD[0:31], LBE[0:3]#,LINT#, LRESETo#, RD/WR#,
MDREQ#/DMPAF/EOT#, TA#, TEA#, TS#, TSIZ[0:1], WAIT#.

LA[2] requires an external pull-up.

M Mode Timing Table Changes

The AC timing for the signals listed in the following table take precedence over the values published in Table 13-8 of the *PCI 9054 Data Book, Version 2.1.*

Signal (Synchronous Outputs) C_L = 50 pF, V_{cc} = 3.0V, T_a = 85 ℃	Clock to Out Worst Case (ns) T_{VALID} (Max) PCI 9054 Revision AC (Data Book Addendum r2.2)	Clock to Out Worst Case (ns) T_{VALID} (Max) PCI 9054 Revision AB (Data Book v2.1)
BDIP#	13.2	10.5
LA[0:31]	10.2	10.0
DMPAF	N/A*	13.0
TEA#	9.3	8.5

* ***Note:*** *The DMPAF signal is an asynchronous signal; therefore, it will be caught on the next clock edge.*

LOCAL BUS OPERATION (M mode (MPC860))

Burst-4 Lword Mode
If the Burst Mode bit is enabled and the Bterm Mode bit is disabled, bursting can start only on a 16-byte boundary and continue up to the next 16-byte address boundary.
After data before the boundary is transferred, the PCI 9054 asserts a new Address cycle (TS#).

DIRECT DATA TRANSFER MODES
The PCI 9054 supports three direct transfer modes:
• **PCI Initiator =** Local CPU (060) accesses PCI memory or I/O.
• **PCI Target =** PCI Master accesses Local memory (SDRAM) or I/O (ST-RAM).
• **DMA =** PCI 9054 DMA controller reads/writes PCI memory to/from Local memory (SDRAM & ST-RAM).

Local Bus Arbitration
The PCI 9054 asserts BR# to request the Local Bus. It owns the Local Bus when BG# is asserted. Upon receiving BG#, the PCI 9054 waits for BB# to de-assert. The PCI 9054 then asserts BB# at the next rising edge of the Local clock after acknowledging BB# is de-asserted (no other device is acting as the Local Bus Master). The PCI 9054 continues to assert BB# while acting as the Local Bus Master (*that is*, it holds the bus until instructed to release BB#) **when the Local Bus Latency Timer is enabled and expires (MARBR[7:0])** or the transaction is complete.
*Note: The Local Bus Pause Timer applies only to DMA operation. It does **not** apply to PCI Target operation.*

Wait States—Local Bus
In PCI Initiator mode, when accessing the PCI 9054 registers, the PCI 9054 acts as a Local Bus Slave. The PCI 9054 asserts external wait states with the TA# signal.
In PCI Target and DMA modes, the PCI 9054 acts as a Local Bus Master. The Internal Wait States bit(s) (LBRD0[21:18, 5:2], (LBRD1[5:2]), DMAMODE0[5:2], and/or DMAMODE1[5:2]) can be used to program the number of internal wait states between the first address-to-data (and subsequent data-to-data in Burst mode).
In PCI Target and DMA modes, if TA# is enabled and active, it continues the Data transfer, regardless of the wait state counter.

RESPONSE TO FIFO FULL OR EMPTY

Table lists the PCI 9054 response to full and empty FIFOs.

Mode	Direction	FIFO	PCI Bus	Local Bus
PCI Initiator Write	Local-to-PCI	Full	Normal	De-assert TA#, RETRY#[1]
		Empty	De-assert REQ# (off the PCI Bus)	Normal
PCI Initiator Read	PCI-to-Local	Full	De-assert REQ# or throttle IRDY#[2]	Normal
		Empty	Normal	De-assert TA#
PCI Target Write	PCI-to-Local	Full	Disconnect or throttle TRDY#[3]	Normal
		Empty	Normal	De-assert BB#[4]
PCI Target Read	Local-to-PCI	Full	Normal	De-assert BB#[4]
		Empty	Throttle TRDY#[3]	Normal
DMA	Local-to-PCI	Full	Normal	De-assert BB#[4]
		Empty	De-assert REQ#	Normal
	PCI-to-Local	Full	De-assert REQ#	Normal
		Empty	Normal	De-assert BB#[4]

1. Issue RETRY# depends upon the PCI Initiator Write FIFO Almost Full RETRY# Output Enable bit (LMISC[6]).
2. Throttle IRDY# depends upon the PCI Initiator PCI Read Mode bit (DMPBAM[4]).
3. Throttle TRDY# depends upon the PCI Target Write Mode bit (LBRD0[27]).
4. BB# de-assert depends upon the Local Bus PCI Target Release Bus Mode bit (MARBR[21]).

DMA OPERATIONS

The PCI 9054 supports two independent DMA channels capable of transferring data from the:
• Local-to-PCI Bus
• PCI-to-Local Bus
Each channel consists of a DMA controller and a dedicated, bidirectional FIFO. Both channels support Block transfers, and Scatter/Gather transfers, with or without End of Transfer (EOT#). Only DMA Channel 0 supports Demand mode

DMA transfers. Master mode must be enabled with the Master Enable bit (PCICR[2]) before the PCI 9054 can become a PCI Bus Master. In addition, both DMA channels can be programmed to:

• Operate in 8-, 16-, or 32-bit Local Bus width
• Use zero to 15 internal wait states (Local Bus)
• Enable/disable internal wait states (Local Bus)
• **Enable/disable Local Bus Burst capability**
• Limit Local Bus bursts to four (BTERM# enable/disable)
• Hold Local address constant (Local Target is FIFO) or increment
• Perform PCI Memory Write and Invalidate (command code = Fh) or normal PCI Memory Write (command code = 7h)
• Pause Local transfer with/without BLAST# (DMA Fast/Slow termination)
• Assert PCI interrupt (INTA#) or **Local interrupt (LINT#)** when DMA transfer is complete or Terminal Count is reached during Scatter/Gather DMA mode transfers
• Operate in DMA Clear Count mode (only if the descriptor is in Local memory)

The PCI 9054 also supports PCI Dual Address with the upper 32-bit registers (DMADAC0 and DMADAC1).
The Local Bus Latency Timer determines the number of Local clocks the PCI 9054 can burst data before relinquishing the Local Bus. The Local Pause Timer sets how soon the DMA channel can request the Local Bus.

RETRY CAPABILITY

PCI Initiator Write FIFO Full
The PCI 9054 supports the PCI Initiator Write FIFO full condition. When enabled (LMISC[6]=1), the PCI 9054 asserts the RETRY# signal to the Local Bus Master to relinquish ownership of the bus and return to finish the initial write at a later time.
Otherwise, the PCI Initiator Write transfer goes through successfully.

If FIFO Almost Full Retry is disabled (LMISC1[6]=0), the PCI 9056 de-asserts TA# (and does not assert RETRY#) until there is space in the FIFO for additional Write data.

PCI Initiator Delayed Read
The PCI 9054 supports Deferred PCI Initiator Read transactions. When the PCI Initiator Deferred Read Enable bit is set (LMISC[4]=1), the PCI 9054 asserts RETRY# and prefetches Read data every time the Local Master requests a read. During a PCI data prefetch, the Local Master is capable of doing other transactions and free to return for requested data at a later time.

Author note : The 060 is not a pipelined command CPU and is only able to retry the previous cycle. It cannot go back to get the result of a posted command.

When Deferred PCI Initiator Read mode is disabled, the Local Master must "keep" the Local Bus and wait for the requested data (TA# is not asserted until data is available to the Local Bus).

Author note : The Retry signal does not exist on 060 protocol. To request a RETRY bus operation to 060, TA# AND TEA# must be inserted in the same clock cycle. The CTPCI logic glue will provides this function.

BUS ERROR

TEA# output

A TEA# interrupt can be asserted if the following occurs:
• PCI Bus Target Abort bit is set (PCISR[11]=1) or Received Master Abort bit is set (PCISR[13]=1)
• Detected Parity Error bit is set (PCISR[15]=1)
• PCI Initiator Local Data Parity Check Error Status bit is set (INTCSR[7]=1) – **NOT SUPPORTED ON CTPCI**
• Messaging Outbound Free queue overflows
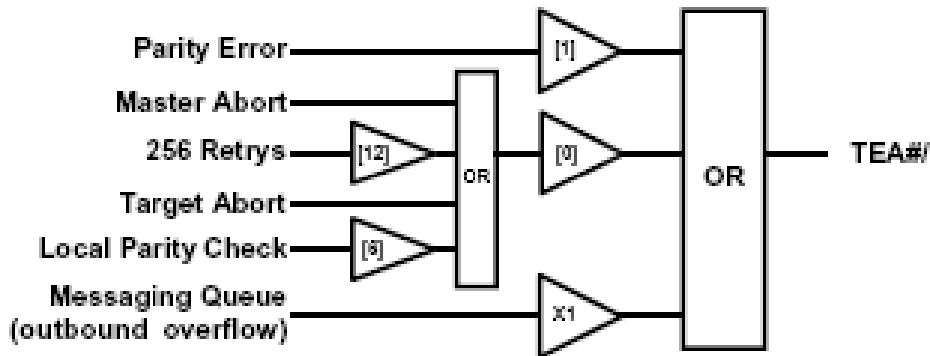
X1 = Outbound Free Queue Overflow Interrupt Full and Mask bits (QSR[7:6]) :
Default value of enable bit (#6) is 1 = activated.

The numbers 0, 1, 6 & 12 represent bit numbers in the INTCSR register :
The bits 0,1 & 12 must be set to 1 to enable the respective sources of TEA
Bit 6 must not be set because local parity is not managed on CTPCI !

Depending upon the error/abort condition and when it is detected, TEA# will either be asserted during the currently active local bus transfer or when the Local Master returns to attempt a new Direct Master Read/Write, Configuration Read/Write, or resumes a Deferred Read.
TEA# will be asserted, regardless of the Deferred Read Enable bit (LMISC[4]) setting.
The PCI 9054 can assert TEA# any time during the transfer, following the clock period during which TS# was asserted.

Author Note : TEA# can be inserted at any time. The 060 protocol bus is not same than PowerPC : if TEA# is inserted with TA#, the 68060 will recognize a RETRY cycle instead of a BUS ERROR. The CTPCI logic glue filters the TA# signal if TEA# is inserted.

TEA# input

The PCI 9054 tolerates TEA# input assertion only during PCI Target or DMA transactions (PCI to CT60 transactions). Only the CT60 watchdog can deliver a TEA# if the hardware on CT60 did not answered after 32us.

The PCI 9054 does not sample TEA# assertion during PCI Initiator transactions.

INTERRUPTS

Local Interrupt Output (LINT#)

The PCI 9054 Local Interrupt (LINT#) output can be asserted by one of the following :
• PCI-to-Local Doorbell/Mailbox register access – **NOT possible on CTPCI**
• PCI BIST interrupt – **NOT possible on CTPCI**
• DMA Ch 0/Ch 1 Done interrupt
• DMA Ch 0/Ch 1 Terminal Count is reached
• DMA Abort Interrupt or Messaging Outbound Post Queue is not empty

The Local Interrupt Input Enable bit must be disabled (INTCSR[11]=0) when LINT# output is active.
LINT# input mode is not supported on CTPCI.

LINT#, or individual sources of an interrupt, can be enabled or disabled with the PCI 9054 Interrupt Control/Status register (INTCSR). This register also provides interrupt status for each interrupt source.
The PCI 9054 Local interrupt is a level output. Interrupts can be cleared by disabling the Interrupt Enable bit of a source or by clearing the cause of an interrupt.
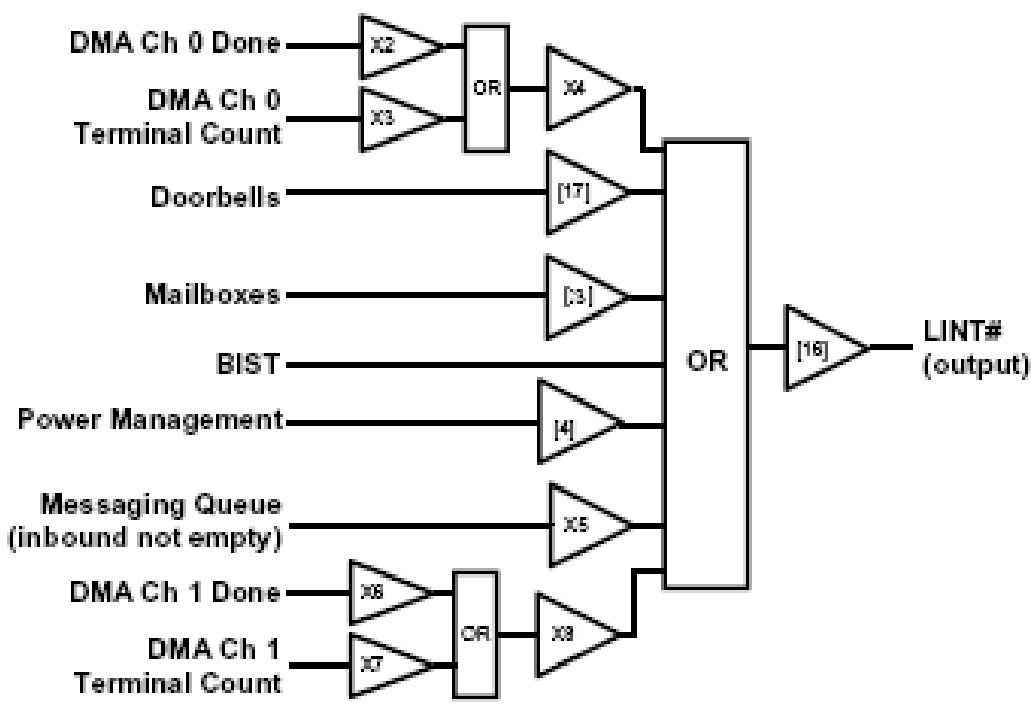
X2 = Channel 0 Done Interrupt Enable bit (DMAMODE0[10]).
X3 = Channel 0 Interrupt after Terminal Count bit (DMADPR0[2]).
X4 = Local DMA Channel 0 Interrupt Enable bit (INTCSR[18]) and DMA Channel 0 Interrupt Select bit (DMAMODE0[17]).
X5 = Inbound Post Queue Interrupt Not Empty and Inbound Post Queue Interrupt Mask bits (QSR[5:4]).
X7 = Channel 1Interrupt after Terminal Count bit (DMADPR1[2]).
X6 = Channel 1 Done Interrupt Enable bit (DMAMODE1[10]).
X8 = Local DMA Channel 1 Interrupt Enable bit (INTCSR[19]) and DMA Channel 1 Interrupt Select bit (DMAMODE1[17]).

The numbers 3, 4, 16 & 17 represent bit numbers in the INTCSR register :
  - Power management is not supported on CTPCI (bit #3)
  - Bit #4 should be set to 1 if Mailboxes are used.
  - **Default value of bit #16 = 1 (LINT# enable).**
  - Bit #17 should be set to 1 if Doorbells are used.

A DMA channel can assert a Local Bus interrupt when done (transfer complete) or after a transfer is complete for the current descriptor in Scatter/Gather DMA mode.
The Local processor can read the DMA Channel 0 Interrupt Active bits to determine whether a DMA Channel 0 (INTCSR[21]) or DMA Channel 1 (INTCSR[22]) interrupt is pending.

The Channel Done bit(s) (DMACSR0[4] and/or DMACSR1[4]) can be used to determine whether an interrupt is one of the following :
• DMA Done interrupt
• Transfer complete for current descriptor interrupt

The Done Interrupt Enable bit(s) (DMAMODE0[10] and/or DMAMODE1[10]) enable a Done interrupt.
In Scatter/Gather DMA mode, a bit in the Next Descriptor Pointer register of the channel (loaded from Local memory)
specifies whether to assert an interrupt at the end of the transfer for the current descriptor.
A DMA Channel interrupt is cleared by the Channel Clear Interrupt bit(s) (DMACSR0[3]=1 and/or DMACSR1[3]=1).

CTPCI INT
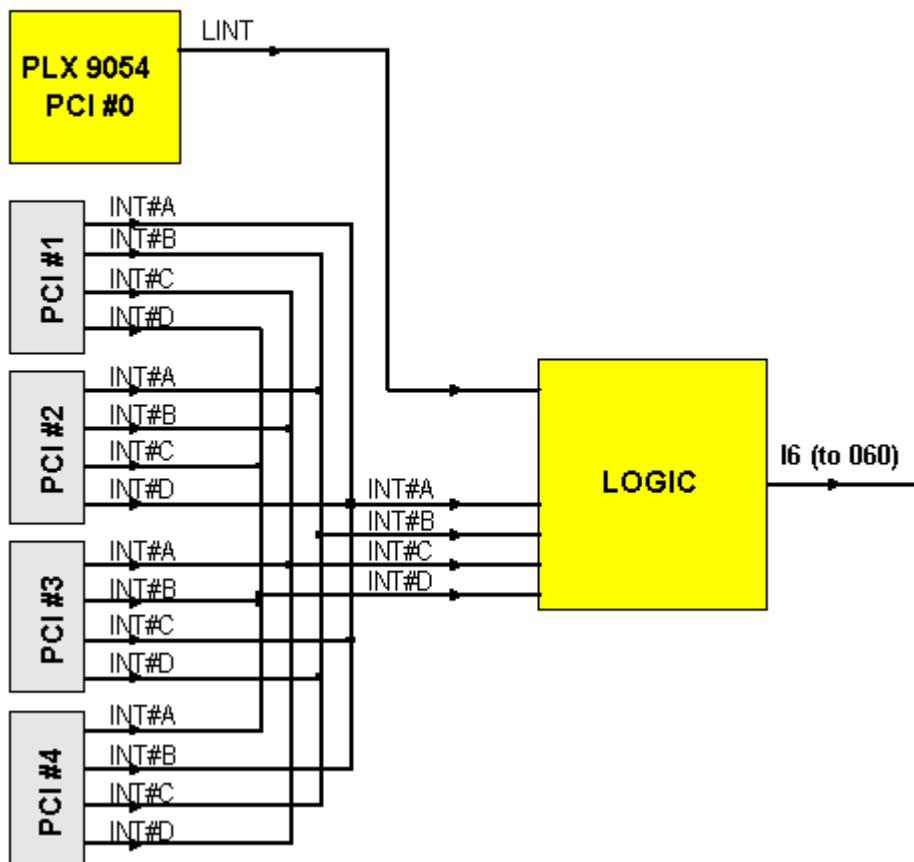
INT (level 6)	VECTOR
LINT	$x9
INT#A	$xA
INT#B	$xB
INT#C	$xC
INT#D	$xD

PCI DEVICES ID

PCI Bridge   IDSEL = 20
PCI slot#1   IDSEL = 21
PCI slot#2   IDSEL = 22
PCI slot#3   IDSEL = 23
PCI slot#4   IDSEL = 24

CPLD REGISTERS

INT VECTOR Register
Byte Write to $E0000003
No Read

Data bits	Name	Default Value	Function
0	x	x	Not used – write 0 for future hardware
1	x	x	Not used – write 0 for future hardware
2	x	x	Not used – write 0 for future hardware
3	x	x	Not used – write 0 for future hardware
4	VE4	0	Int. Vector address bit#4
5	VE5	0	Int. Vector address bit#5
6	VE6	0	Int. Vector address bit#6
7	VE7	0	Int. Vector address bit#7

Enable INT Register
Byte Write to $E0000001
Byte/word Read

Data bits	Name	Default Value	Function
0	ENBIP	0	ENaBle INT PLX
1	ENBIA	0	ENaBle INT #A
2	ENBIB	0	ENaBle INT #B
3	ENBIC	0	ENaBle INT #C
4	ENBID	0	ENaBle INT #D
5	x	x	Not used – write 0 for future hardware
6	x	x	Not used – write 0 for future hardware
7	x	x	Not used – write 0 for future hardware

INT PEND Register
Byte/word Read at $E0000000
No Write

Data bits	Name	Inactive Value	Function
0	INTP	0	INT PLX
1	INTA	0	INT #A
2	INTB	0	INT #B
3	INTC	0	INT #C
4	INTD	0	INT #D
5	x	x	Not used – write 0 for future hardware
6	x	x	Not used – write 0 for future hardware
7	x	x	Not used – write 0 for future hardware

Misc. Register
Byte Write to $E0000023.

Data bits	Name	Default Value	Function
0	PCIRST	0	Set to 1 : Reset the PLX, the PCI slots & the PCI arbiter.
1	ITF	0	Set to 1 : Fast IDE timings for 75-100 Mhz clocks
2	x	x	Not used – write 0 for future hardware
3	x	x	Not used – write 0 for future hardware
4	x	x	Not used – write 0 for future hardware
5	x	x	Not used – write 0 for future hardware
6	x	x	Not used – write 0 for future hardware
7	x	x	Not used – write 0 for future hardware

Note : This register is used by software to test the CTCPI presence.
Write to $E0000020 : if bus error -> no CTPCI

CTPCI board to PCI slots board cables

There are 2 ribbon cables between the CTPCI main board and the PCI connectors board.

The two cables are made with ATA 80 wires standart cables.

It is necessary using the system and master ends of the flat ATA cables. The middle (slave) connector of the flat cable cannot be used. So it is not possible to cut the flat cable to reduce the length using system and slave ends.

Cable #1 (connecteur J5)

Pin #	Signal Function	Pin #	Signal Function
1	INTA#	2	Ground
3	INTC#	4	INTD#
5	GNT1#	6	REQ1#
7	REQ2#	8	CLK3
9	CLK4	10	GNT4
11	AD30	12	AD29
13	AD26	14	AD25
15	AD23	16	AD22
17	AD19	18	AD18
19	Ground	20	Key
21	C/BE2#	22	Ground
23	IRDY#	24	Ground
25	DEVSEL#	26	Ground
27	LOCK#	28	PERR#
29	C/BE1#	30	Ground
31	AD14	32	AD13
33	AD10	34	NC
35	AD8	36	C/BE0#
37	AD5	38	AD4
39	AD1	40	Ground

Cable #2 (connecteur J6)

Pin #	Signal Function	Pin #	Signal Function
1	INTB#	2	Ground
3	RST#	4	CLK1
5	CLK2	6	GNT2#
7	GNT3#	8	REQ3#
9	REQ4#	10	AD31
11	AD28	12	AD27
13	AD24	14	C/BE3#
15	AD21	16	AD20
17	AD17	18	AD16
19	Ground	20	Key
21	FRAME#	22	Ground
23	TRDY#	24	Ground
25	STOP#	26	Ground
27	SERR#	28	PAR
29	AD15	30	Ground
31	AD12	32	AD11
33	AD9	34	NC
35	AD7	36	AD6
37	AD3	38	AD2
39	AD0	40	Ground

3. Delayed Read Mode bit (MARBR[24])

Changes to PCI 9054 Data Book revision 2.1: The name for the Mode/DMA Arbitration register bit 24 (MARBR[24]) is changed from "Delayed Read Mode" to "PCI r2.1 Features Enable". PCI 9054 Data Book sections 3.4.3.2 for M mode, and the MARBR[24] register bit description, are revised as follows:

Table 4-35. (MARBR; PCI:08h or ACh, LOC: 88h or 12Ch)
Mode/Arbitration Register

Bit	Description	Read	Write	Value after Reset
24	**PCI r2.1 Features Enable.** When set to 1, the PCI 9054 performs all PCI Read and Write transactions in compliance with PCI r2.1. Setting this bit enables Delayed Reads, 2^{15} PCI Clock timeout on Retries, 16- and 8-clock PCI latency rules, and enables the option to select PCI Read No Write Mode (Retries for writes) (bit [25]). Refer to Sections 3.4.3.2 and 5.4.2.2 for additional information. Value of 0 causes TRDY# to remain de-asserted on reads until Read data is available. If Read data is not available before the PCI Target Retry Delay Clocks counter (LBRD0[31:28]) expires, a PCI Retry is issued.	Yes	Yes	0

3.4.3.2 PCI r2.1 Features Enable
The PCI 9054 can be programmed through the PCI r2.1 Features Enable bit (MARBR[24]) to perform all PCI Read/Write transactions in compliance to PCI r2.1 (and PCI r2.2). The following PCI 9054 behavior occurs when MARBR[24] = 1.

3.4.3.2.1 Direct Slave Delayed Read Mode
PCI Bus single cycle aligned or unaligned 32-bit Direct Slave Read transactions always result in a 1-Lword single cycle transfer on the Local Bus, with corresponding Local Address and TSIZ[0:1] asserted to reflect the PCI Byte Enables (C/BE[3:0]#), unless the PCI Read No Flush Mode bit is enabled (MARBR[28] = 1) (refer to Section 3.4.3.3). This causes the PCI 9054 to Retry all PCI Bus Read requests that follow, until the original PCI Address and Byte Enables (C/BE[3:0]#) are matched.

3.4.3.2.2 2_{15} PCI Clock Timeout
If a PCI Master does not complete its originally requested Direct Slave Delayed Read transfer, the PCI 9054 flushes the Direct Slave Read FIFO after 2_{15} PCI clocks and will grant an access to a new Direct Slave Read access. The PCI 9054 Retries all other Direct Slave Read accesses that occur before the 2_{15} PCI clock timeout.

3.4.3.2.3 PCI r2.1 16- and 8- clock rule
The PCI 9054 guarantees that if the first Direct Slave Write data cannot be accepted by the PCI 9054 and/or the first Direct Slave Read data cannot be returned by the PCI 9054 within 16 PCI clocks from the beginning of the Direct Slave cycle (FRAME# asserted), the PCI 9054 issues a Retry (STOP# asserted) to the PCI Bus.
During successful Direct Slave Read and/or Direct Slave Write accesses, the subsequent data after the first access is accepted for writes or returned for reads in 8 PCI clocks (TRDY# asserted). Otherwise, the PCI 9054 issues a PCI disconnect (STOP# asserted) to the PCI Master.
In addition, setting the PCI r2.1 Features Enable bit (MARBR[24] = 1) allows optional enabling of the following PCI r2.1 function:
  • No write while delayed read is pending (PCI Retries for writes) (MARBR[25])

The following PCI 2.1 optional function can be activated except if MARBR[25,24] = 11b:
  • Write and flush pending delayed read (MARBR[26])

9. Retried Direct Slave Single Read completed as Burst Read

Design Issue: If a Direct Slave Single Read request that has been retried by the PCI 9054 is completed as a Burst Read transaction, the PCI 9054 will stall the PCI bus with continuous retries on the second read data. If the PCI r2.1 Features Enable bit is set (MARBR[24] = 1), the PCI 9054 will issue a Target Abort following expiration of 32K PCI clock timeout. If this bit is clear (MARBR[24] = 0), the 32K PCI clock discard timer is not enabled.

The PCI Specification does not allow a PCI master to extend a read transaction beyond its original intended length after it has been terminated with Retry. Accordingly, the scenario described above can only occur if a second PCI master requests the same transaction (address, command, byte enables and parity) that is being retried for the original PCI master request. The PCI 9054 cannot and need not distinguish between the two and will simply attempt to complete the access.

Solutions/Workarounds: To avoid stalling the PCI bus under this scenario:

1. Set the PCI r2.1 Features Enable bit (MARBR[24] = 1) to enable 32K PCI clock timeout for retries.

2. Enable both the Read Ahead Mode feature (MARBR[28] = 1) and local Prefetch (LBRD0[8] = 0 for Space 0, LBRD1[9] = 0 for Space 1, and/or LBRD0[9] = 0 for Expansion ROM). This will allow the PCI 9054 to keep the read data in the FIFO and transfer it on the PCI request.

   This workaround is only applicable to memory-mapped address spaces. Although burst I/O transactions are legal in PCI, processors typically do not perform burst I/O and x86 processors cannot. Additionally the PCI 9054 will disconnect with the first data of a PCI I/O transaction. The PCI 9054 does not prefetch I/O-mapped address spaces, and therefore Read Ahead mode is not applicable to I/O-mapped spaces.

3. Limit the number of retries allowed from the PCI 9054 before discarding an uncompleted transaction and reporting retry timeout error.

13. PCI Target Abort during DMA Transfer

Design Issue: During a PCI-to-Local DMA transfer, if a Target Abort occurs on the last DMA data transfer cycle, the PCI 9054 will generate an unknown data cycle for the last data to the Local bus. A PCI Target Abort at any other time during the DMA transaction will be successfully completed. This is a rare case condition. If a Target Abort during a DMA transaction occurs, the system should repeat the operation.

Recommendation: A Target Abort is by definition an error condition, and if a Target Abort occurs the last data should be assumed to be invalid. After a DMA transaction is complete, software should check the Received Target Abort status bit (PCISR[12]). If the bit indicates that a PCI Target Abort occurred, software should repeat the DMA transaction.

14. Interrupt Control/Status register (INTCSR) indication of a Master Abort or Target Abort condition

Design Issue: When a Master Abort or Target Abort condition is detected, status bits INTCSR[27:24] reflect the most recent error condition depending on the abort received. Clearing the abort condition will not reset these status bits to their default values of 1.

Recommendation: The INTCSR[27:24] status bits indicating that a Master Abort or Target Abort was signaled or detected are updated when either another abort condition occurs, or a PCI reset is applied to the PCI 9054 (a software reset via CNTRL[30] will not change INTCSR register contents). Otherwise, these bits reflect the status of the last abort condition received. If monitoring of these bits is necessary for error recovery, monitor the equivalent PCI configuration register error bits in the PCI Status register (PCISR[13:11]). PCI 9054 issuance of a Master Abort is signaled in PCISR[13], PCI 9054 issuance of a Target Abort is signaled in PCISR[11], and receipt of a Target Abort from another device while PCI 9054 is master is signaled in PCISR[12].

17. Direct Slave Transfer Size

Issue: In PCI 9054 Data Book version 2.1, Table 3-3 lists how data is transferred onto the M-mode Local Bus during Direct Slaves Writes. The table is incorrect and is replaced by the Table 3-3 shown below.

Table 3-3. Data Bus TSIZ[0:1] Contents for Single Write Cycles

Transfer Size	TSIZ [0:1]		Address		32-Bit Port Size				16-Bit Port Size		8-Bit Port Size
			LA30	LA31	LD[0:7]	LD[8:15]	LD[16:23]	LD[24:31]	LD[0:7]	LD[8:15]	LD[0:7]
Byte	0	1	0	0	OP0	—	—	—	OP0	—	OP0
	0	1	0	1	—	OP1	—	—	—	OP1	OP1
	0	1	1	0	—	—	OP2	—	OP2	—	OP2
	0	1	1	1	—	—	—	OP3	—	OP3	OP3
Word	1	0	0	0	OP0	OP1	—	—	OP0	OP1	—
	1	0	1	0	—	—	OP2	OP3	OP2	OP3	—
Lword	0	0	0	0	OP0	OP1	OP2	OP3	—	—	—

Note: The "—" symbol indicates that a valid byte is not required during that Write Cycle.
However, the PCI 9054 drives these byte lanes, although the data is not used.

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May 2005

2. Simultaneous Access to Queue Register in Messaging Unit

Erratum Issue: The PCI 9054 updates one of four queue pointers automatically each time there is a Read or Write to the messaging unit Inbound (Port 40h) or Outbound (Port 44h) ports. The four registers are the inbound free tail pointer (IFTPR), the inbound post head pointer (IPHPR), the outbound free head pointer (OFHPR), and outbound post tail pointer (OPTPR). If a local master initiates a write to the PCI 9054 messaging unit queue registers simultaneous to a PCI access to the Inbound or Outbound ports, the PCI 9054 will fail to automatically increment the appropriate pointers to reflect this. This can result in overwriting a previous message or retrieving a previously read message from the queue. These pointers cannot be 'corrected' due to the fact that the IOP cannot determine if an increment failure has occurred. The failure only occurs when the PCI 9054 returns READY#/TA# to the local master simultaneous with the PCI 9054 returning TRDY# to the PCI master on an Inbound or Outbound port access that has been retried.

This erratum does not affect the I_2O protocol. It only affects custom messaging unit implementations.

Solutions/Workarounds (use any):

1. Disable the PCI r2.1 Features Enable bit by clearing MARBR[24]. With this bit clear, the PCI Target Retry Delay Clocks register bits (LBRD0[31:28]) should be set to a value of 3h or greater.

2. **For Multiple Initiator Implementations:**

   a. Implement a semaphore using two on-chip mailboxes or any shared memory region, so that the local master can access the messaging unit queue registers only when the PCI master is not accessing them. Use one mailbox to signal that the PCI bus wants to access the messaging unit and the other mailbox to signal that the Local bus wants to access the messaging unit. Before accessing the messaging unit read the status of the opposite side's mailbox. If the other side has access then Backoff (attempt access later) or else write a flag in the mailbox to claim access. Then read the other mailbox to ensure that both the PCI and Local sides did not write their flags simultaneously. If they did each side will need to Backoff, otherwise access the messaging unit and then clear the flag in the mailbox.

   b. Update the interfering queue registers only from the PCI side, via messages passed through the PCI 9054 internal mailbox registers.

   ### For Single Initiator Implementations:

   Implement a single request/reply message protocol for custom message passing. This is recommended for applications where there is a single host and the host waits for a reply before initiating a new request.

3. Direct Master Read with PCI Initiator Cache Enabled

Erratum Issue: PCI 9054 PCI Initiator (Direct Master) reads with PCI Initiator Cache enabled (DMPBAM[2] = 1) will result in 32-bit data reads intermittently returning incorrect data. The incorrect data returned will be the Lword value at the 32-bit aligned address that immediately precedes the correct value. In other words, data that has been previously cached and read out of the PCI Initiator Read FIFO will be repeated on a subsequent read. This erratum occurs in all three local bus modes (C, J, and M).

Solution/Workaround:

Disable PCI Initiator Cache by clearing the PCI Initiator Cache Enable bit (DMPBAM[2] = 0).

5. Cannot Perform a New Read or Write after Backoff – Must Resume with Last Address

Erratum Issue: The PCI 9054 Data Book version 2.1 pages 3-16 and 5-14 states: "A new…read is performed if the resumed Local Bus cycle is not the same as the Backed Off cycle".

When the PCI 9054 BREQo/RETRY# signal is enabled (EROMBA[4] = 1) to back off a Direct Master transaction (to resolve a potential deadlock), if the local master does not resume a backed-off transfer with the originally backed-off

address, the PCI 9054 will incorrectly assert BREQo/RETRY# without asserting LHOLD. If the local master does not apply the correct continuation address, BREQo/RETRY# will be asserted without LHOLD two clocks after the local master asserts ADS#.

Solution/Workaround:

Only resume a backed-off transfer with the continuation address, that is, the Master must resume the backed-off transfer with the address that it was backed-off from.

6. TEA# Pin/Signal Can Be Asserted Improperly

General functional description of proper TEA# assertion

TEA#, Transfer Error Acknowledge, is a wired-OR signal that is asserted by a Slave device on the Local Bus. The CT60 can assert TEA# as a Master or Slave if its Bus Monitor times out. If the Bus Monitor does time out and the CT60 asserts TEA#, the device it is communicating with needs to detect this regardless of its configuration (Master or Slave) and get off the Local bus in one clock cycle. Additionally the device should terminate any active PCI bus activity via an abort and set its status bits/registers appropriately.

Item #1

Erratum Issue: The CT60 can assert TEA# as a Master or Slave if its Bus Monitor times out.

1. If TEA# is asserted by the CT60 while the PCI 9054AC is the local bus master, TEA# will preempt TA# input and terminate the current cycle. If the burst isn't completed, the PCI 9054AC will generate a new TS# and continue. This applies for Direct Slave and DMA transfers. This case is possible if the PCI9054 accesses on CT60 at an address (bad) where there is no hardware answering ($\rightarrow$ BUS ERROR).

2. If TEA# is asserted by the CT60 while the PCI 9054AC is the local bus slave, the PCI 9054AC ignores TEA**#.**

Author note : This case 2 may only be possible if the CT60 watch dog reaches the 32us delay during an access from 060 to the PCI9054 chip.

Solutions/Workarounds (use either):

1. Disable or program CT60 Bus Monitor to a value high enough so that it exceeds the amount of time necessary to get the bus and execute the transfer. This feature is not possible on CT60. Delay is hardware fixed to 32us.

2. Have the CT60 assert the LINT# pin instead of TEA# when the Bus Monitor times out. That will cause the PCI INTA# interrupt pin to assert so that the system can issue a software reset to the local section, by setting the PCI 9054AC CNTRL register bit [30] to 1, and then clearing it after the reset is completed.
Author note : This feature is not actually present on CT60. It may be possible but needs to modify the SDR chip on CT60.

Item #2

Erratum Issue: If a Target Abort is received on any transfer, the PCI 9054AC may continue to drive the LD[0:31] pins for up to 4 cycles after TEA# has been asserted.

Solution/Workaround :

Do not start a new Local bus cycle for at least four clocks after the PCI 9054AC asserts TEA#.
Author note : to be verified !

Item #3

Erratum Issue: TEA# will be improperly asserted by the PCI 9054AC if it is not participating in a Local bus transfer if the two events listed below occur in the following sequence.

1. The BI# (Burst Inhibit) pin is asserted during a Direct Master or IDMA transfer.

2. A PCI Master/Target Abort is detected by the 9054AC when it is not participating in a Local bus transfer.

Solutions/Workarounds (use either)

1. Do not assert the BI# pin during a Direct Master or IDMA transfer.

2. Use the LINT# pin instead of the TEA# pin.

Author note : TEA# must be filtered if no access is started by PLX on local bus.

10. DMA Scatter-Gather Descriptor IRDY# PCI Protocol Violation

Erratum issue: If the PCI 9054 receives a PCI Target Abort when reading a Scatter-Gather DMA descriptor from the PCI bus, the PCI 9054 will immediately float the IRDY# signal, rather than drive the IRDY# signal from active (level 0) to inactive (level 1) for 1 PCI clock period before floating, as is required by the PCI Specification for STS I/O buffer protocol. As a result, it may take several PCI clocks for the IRDY# signal to reach a TTL logic level high.

Solution/Workaround:

No fix is required, and no failures have been observed. The PCI Specification also requires that IDRY# have a pull-up resistor on the motherboard. If the above condition is encountered, adding an external pull-up (in parallel with motherboard pull-up) will decrease the resistance to allow the signal to reach a TTL logic high more quickly.

11. PQFP Package LA[0:5] Signal Noise

Note. This erratum only pertains to the PQFP packaged PCI 9054AC part (PLX part number PCI 9054-AC50PI). It does not pertain to the PBGA packaged part (PLX part number PCI 9054-AC50BI).

Erratum Issue: For the PCI 9054-AC50PI, noise may be injected on the Local Bus causing incorrect values to be output on address bits LA[0:5] if the following occur simultaneously:

1. The PCI 9054-AC50PI is driving the PCI bus with patterns that maximize the number of simultaneously switching outputs on AD[31:0], and

2. The PCI 9054-AC50PI is driving a Local Bus address during Direct Slave or DMA data transfers.

The Local bus signals affected LA[0:5] that should be logic 0's might be incorrectly driven to up to 0.8V for as long as 5 nsec. The amplitude of the noise is proportional to the loading and signal amplitude/charge on the PCI AD[5:0] signals when these are driven low by the PCI 9054. Additionally, only Local Bus devices that detect a logic one near the bottom of the switching range are affected.

Solutions/Workarounds (do one of the following):

1. Do not use the PCI 9054-AC50PI LA[0:5] signals in designs that perform Direct Slave or DMA data transfers. This will limit PCI 9054-AC50PI designs to the lower 64 Mbytes of Local Bus address space

2. Use the PCI 9054-AC50BI or PCI 9056BA66BI parts instead which do not have this issue.

15. Direct Slave Disconnect Without Data

Erratum issue: When the PCI 2.2 Mode bit is set (MARBR[24] = 1), during a Direct Slave burst read, if the first datum is not available for transfer within 16 PCI clocks, the PCI 9054 will issue a PCI Retry, and latch the PCI Command, Address and Byte Enables into its Read FIFO. A PCI master that is target terminated with Retry must unconditionally repeat the same request until it completes.

If instead at least one datum is transferred to the PCI bus, and if the next datum for the PCI burst read is not available within 8 PCI clocks, the PCI 9054 will issue a Disconnect Without Data (TRDY# de-asserted and STOP# asserted, same as Retry signaling). A PCI master that is target terminated with Disconnect is not required to repeat the same request.

The PCI 9054 latches the Command, Address and Byte Enables into its Read FIFO and does not flush the FIFO when issuing a Disconnect Without Data, the same as it does when issuing a Retry (which is a special case of Disconnect Without Data). Therefore, the PCI 9054 requires that the PCI master repeat any transaction that the PCI 9054 terminates with a Disconnect Without Data.

If a PCI Master does not complete its originally requested Direct Slave Delayed Read transfer, the PCI 9054 flushes the Direct Slave Read FIFO after 2^15 PCI clocks and will grant an access to a new Direct Slave Read access. The PCI 9054 retries all other Direct Slave Read accesses that occur before the 2^15 PCI clock timeout.

Typically, if a PCI master receives a Disconnect Without Data in response to its issuance of a read command, the master will repeat the transaction (because the master still wants the data), and the PCI 9054 will respond normally. A situation in which a PCI master might instead read a different address would be an upstream bridge that is 64-bit architecture receiving the Disconnect Without Data on a non-Qword aligned address, with the PCI 9054 Local Address Space being read mapped as Prefetchable (the space's LASxRR[3] and PCIBAR[3] register bits are set). In this case, the bridge might repeat the read starting one address earlier, discarding the last Lword that it read in order to align its repeated read to a Qword-aligned address. The bridge is permitted to discard data only if the target's address space is mapped as Prefetchable memory (LASxRR[3,0] = 10b). It is legal for a bridge to not discard the data but repeat the read starting with the Qword-aligned address with all Byte Enables de-asserted, however, such behavior by design is unlikely.

This erratum does not occur for reads of PCI 9054 registers, and is unlikely to occur for I/O-mapped Local Address Spaces since typical CPUs do not perform burst I/O reads (a Disconnect Without Data can only occur on burst transfers).

Workaround:

Configure memory-mapped Local Address Spaces as non-Prefetchable (LASxRR[3] = 0 in the serial EEPROM). Changing Prefetchable mapping to non-Prefetchable may reduce performance, since the upstream bridge is no longer allowed to prefetch beyond the amount of data that it was commanded to fetch.

IDE port

Pin	Name	Description	Info
1	/RESET	Reset	From CT60/63 Reset signal
2	GND	Ground	
3	DD7	Data 7	From/to CPLD through 56 ohms resistor
4	DD8	Data 8	From/to CPLD through 56 ohms resistor
5	DD6	Data 6	From/to CPLD through 56 ohms resistor
6	DD9	Data 9	From/to CPLD through 56 ohms resistor
7	DD5	Data 5	From/to CPLD through 56 ohms resistor
8	DD10	Data 10	From/to CPLD through 56 ohms resistor
9	DD4	Data 4	From/to CPLD through 56 ohms resistor
10	DD11	Data 11	From/to CPLD through 56 ohms resistor
11	DD3	Data 3	From/to CPLD through 56 ohms resistor
12	DD12	Data 12	From/to CPLD through 56 ohms resistor
13	DD2	Data 2	From/to CPLD through 56 ohms resistor
14	DD13	Data 13	From/to CPLD through 56 ohms resistor
15	DD1	Data 1	From/to CPLD through 56 ohms resistor
16	DD14	Data 14	From/to CPLD through 56 ohms resistor
17	DD0	Data 0	From/to CPLD through 56 ohms resistor
18	DD15	Data 15	From/to CPLD through 56 ohms resistor
19	GND	Ground	
20	KEY	Key	
21	n/c	Not connected	
22	GND	Ground	
23	/IOW	Write Strobe	From CPLD through 56 ohms resistor
24	GND	Ground	
25	/IOR	Read Strobe	From CPLD through 56 ohms resistor
26	GND	Ground	
27	IO_CH_RDY	Not used	To CPLD
28	n/c	Not connected	
29	n/c	Not connected	
30	GND	Ground	
31	IRQ	Interrupt Request	To Falcon IDE IRQ signal
32	n/c	Not connected	
33	DA1	Address 1	From CT60/63 ADD bus through 56 ohms resistor
34	n/c	Not connected	
35	DA0	Address 0	From CT60/63 ADD bus through 56 ohms resistor
36	DA2	Address 2	From CT60/63 ADD bus through 56 ohms resistor
37	/CS0	(1F0-1F7)	From CPLD through 56 ohms resistor
38	/CS1	(3F6-3F7)	From CPLD through 56 ohms resistor
39	IDE_ACT	Not used	
40	GND	Ground	