DHG
Déesse Hardware Guide

Rev. 1.6 – © Rodolphe Czuba - May, the 30th, 2000

This guide is intended for hardware and software developers. It is not a complete documentation about the chips used by the card. For a complete technical information, please refer to the DSP56301 User's Manual (DSP56301UM/AD), the DSP56300 Familly Manual (DSP56300FM/AD REV2) and the TLC320AD77C Data Manual (TI Doc# SLAS194).

1- DEESSE OVERVIEW

Déesse is a DSP + High Quality AUDIO PCI card designed for all PCI computers.
It supports the **PCI 2.1 protocole at 33 MHz** with 3.3V I/O (LVTTL) with 5V tolerance.

It is based on two sub-systems :

- a DSP system based on the **MOTOROLA DSP56301**.
- an AUDIO system based on the **TEXAS INSTRUMENT TLC320AD77C**

The **DSP56301** is based on the powerful DSP Engine DSP56301 Core capable of **executing an instruction on every clock cycle**, thus yielding a twofold performance increase as compared to the 56000 Core while **maintaining object code compatibility with it.**
The **TLC320AD77C** is a cost competitive stereo analog-to-digital (A/D) and digital-to-analog (D/A) **24-Bit delta-sigma** converter for consumer applications with demand excellent audio performances such as mini-disks, audio/video receivers, musical intruments, and other end-equipments requiring high performance digital audio conversion.
It has a wide variety of serial inputs options for **16-, 20-, or 24-Bit input/output data**.
It has an extremely wide range of sampling rates starting at **16 kHz and increasing upwards to 96 kHz**.
Its internal bandgap design provides a very clean voltage reference.

1.1- DEESSE features

- DSP56301 at **100MHz (100 Mips)**
- 8 KWords (24KBytes) of internal memory (X, Y & P)
- **128KWords (384Kbytes)** of SRAM (10ns) as external DSP¨memory (X,Y & P).
- Stereo Audio Sampling at **22.05, 24, 32, 44.1, 48, 64, 88.2, 96 kHz**
- Stereo Audio Sampling in **16-, 20-, or 24-Bit formats**
- Two CINCH for Stereo **Audio Input** with **0.7 Vrms Input**.
- Two CINCH for Stereo **Audio Output** with **0.7 Vrms Output**.
- One **DSP LINK connector** for external connections of hardware such like **multi-CODEC, AES-EBU, S/PDIF and Data aquisition Boxes or 19' Racks**.
- Several 1A power supplies (+3.3V / +5V / +12V / -12V) protected by fuses and filtered for EMI compliance.
- 32-Bit / 33 MHz **PCI** 2.1 interface
- 3.3V design

1.2- DSP 56301 features used by Déesse

High performance DSP56300 Core

- 100 Million instructions per second (Mips) with a 100 MHz clock
- Object code compatible with the 56K Core
- Fully pipelined 24 x 24 Bit Parallel Multiplier-Accumulator
- 56 Bit Parallel Barrel Shifter
- 16 Bit Arithmetic Support

- Highly Parallel Instruction Set
- Position Independent Code (PIC) support
- Unique DSP Addressing Modes
- On-Chip Memory-Expandable Hardware Stack
- Nested Hardware Do Loops
- Fast Auto-Return Interrupts
- On-Chip Concurrent Six-Channel DMA Controller
- On-Chip PLL

On-Chip Memories
- On-Chip 2048 x 24 Bit X Data RAM
- On-Chip 2048 x 24 Bit Y Data RAM
- On-Chip 3072 x 24 Bit Program RAM
- On-Chip 1024 x 24 Bit Instruction Cache/Program RAM
- On-Chip 192 x 24 Bit Bootstrap ROM

Off-Chip Memory
- 384 KBytes/128 KWord (24-Bit) of 10ns SRAM

On-Chip Peripherals
- 32-Bit PCI 2.1 interface
- Two Enhanced Synchronous Serial Interface (ESSI)
- Serial Communication Interface (SCI) with Baud Rate Generator
- Triple Timer Module

Reduced Power Dissipation
- Very low power CMOS design
- Wait and Stop low power standby modes
- Fully-static logic, operation frequency down to 0 MHz
- Power Management special circuitry

1.3- TI CODEC TLC320AD77C features used by Déesse

24-Bit Delta Sigma Stereo ADC and DAC:
- **16-, 20-, or 24-Bit Input/Output Data**
- Sampling Rates : **22.05, 24, 32, 44.1, 48, 64, 88 and 96 kHz**
- Master Clock: 256 fs or 384 fs
- 3.3-V Power Supply Operation
- Internal Bandgap Voltage Reference

Stereo ADC:
- Differential Input
- 128x Oversampling
- **High Performance: 100-dB Signal-to-Noise Ratio (SNR) (EIAJ), 100-dB Dynamic Range**
- Digital High-Pass Filter

Stereo DAC:
- Single-Ended Output
- 128x Oversampling
- **High Performance: 100-dB Signal-to-Noise Ratio (SNR) (EIAJ), 100-dB Dynamic Range**

Special Features:
- High Jitter Tolerance
- Good Phase Characteris tics
- Excellent Power Supply Rejection Ratio

2- DSP LINK Connector

It is managed by the ESSI#0 high speed port of the DSP (ESSI#1 port is used for the CODEC link and configuration).

The DSP LINK port uses a standart HE13 male 2x13 pin connector on Déesse that has to be prolongated out of the machine by a standart parallel port with backpanel metal bracket (DB25 connector + 26 wires ribbon cable).

Pinout of the DSP LINK : Déesse HE13 Male connector

SC2/LRCK0	1	2	GND
SC01	3	4	GND
SC00	5	6	GND
STD0	7	8	GND
SCK0	9	10	GND
SRD0	11	12	GND
TXD	13	14	GND
SCLK	15	16	GND
RXD	17	18	GND
TIO0	19	20	GND
TIO1	21	22	-12V / 1A
+3.3V / 1A	23	24	+12V / 1A
+5V / 1A	25	26	nc

Pinout of the DSP LINK : DB25 Backpanel Female connector – External view

SC2/LRCK	1	14	GND
SC1	2	15	GND
SC0	3	16	GND
STD	4	17	GND
SCK	5	18	GND
SRD	6	19	GND
TXD	7	20	GND
SCLK	8	21	GND
RXD	9	22	GND
TIO0	10	23	GND
TIO1	11	24	-12V / 1A
+3.3V / 1A	12	25	+12V / 1A
+5V / 1A	13		

This DSP LINK port provides three different ports and four power supplies.

- ESSI port uses the signals SC2/LRCK, SC1, SC0, STD, SCK and SRD.
- SCI port uses the signals TXD, SCLK and RXD.
- TIO port uses the signals TIO0 and TIO.1
- **Power supplies of +3.3V, +5V, +12V and –12V are available with a current up to 1 A.**
These four power sources are protected with a 1 Ampere fuse.

All the signals and power lines are EMI filtered with Ferrite Bead.

Be carefull to not confuse SCK (of ESSI) and SCLK (of SCI) !

2.1- Enhanced Synchronous Serial Interface (ESSI)

There are two independent and identical Synchronous Serial Interfaces in the DSP56301 :
ESSI#0 used for the DSP LINK and ESSI#1 used for the CODEC.

The **E**nhanced **S**ynchronous **S**erial **I**nterface (ESSI) provides a full-duplex serial port for serial communication with a variety of serial devices including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals wich implement the Motorola SPI. The ESSI consists of independent transmitter and receiver sections and a common ESSI clock generator.

This interface is named synchronous because all serial tranfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is similar in that it is also intended for periodic transfers; however, it will support up to 32 words (time slots) per period. This mode can be used to build **Time Division Multiplexed (TDM) networks.** In contrast, the on-demand mode is intended for non periodic transfers of data. This mode can be used to transfer data serially at high speed when the data becomes available. This mode offers a subset of the SPI protocol.

Three to six pins are required for operation, depending on the operating mode selected.
STD, SC0, SC1 are fully synchronized if they are programmed as transmit data pins.

Serial Transmit Data pin (STD)

STD is used for transmitting data from TX0 serial transmit shift register. STD is an output when data is being transmitted from TX0 shift register. With an internally generated bit clock, the STD becomes high impedance after the last data bit has been transmitted for a full clock period, assuming another data word does not follow immediately. If a data word follows immediately, there will not be a high-impedance interval.

STD may be programmed as a general-purpose pin (PC5) when the ESSI STD funtion is not being used.

Serial Receive Data pin (SRD)

SRD receives serial data and tranfers the data to the ESSI receive shifter.

SRD may be programmed as a general-purpose I/O pin (PC4) when the ESSI SRD function is not being used.

Serial Clock pin (SCK)

SCK is a bidirectional pin providing the serial bit rate clock for the ESSI interface. The SCK is a clock input or output used by all the enabled transmitters and receiver in synchronous modes or by all the enabled transmitters in asynchronous modes.

SCK may be programmed as a general-purpose I/O pin (PC3) when the ESSI SCK function is not being used.

NOTE : Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of three CLKOUT cycles time. (i.e., the DSP56301 clock frequency must be at least three times the external ESSI clock frequency and each ESSI phase must exceed the minimum of 1.5 CLKOUT cycles) :
for a DSP at 100 MHz, the maximum SCK frequency is 100/3 = 33.33 MHz.

Serial Control 0 pin (SC0)

The function of this pin is determined by the selection of either synchronous or asynchronous mode.
For asynchronous mode, this pin will be used for the receive clock I/O.
For synchronous mode, this pin is used for transmitter data out pin of transmit shift register number 1 or for serial flag I/O.
A typical application of flag I/O would be multiple device selection for addressing in codec systems. If this pin is configured as serial flag pin, its direction is determined by the SCD0 bit in the CRB.

When configured as an output, this pin pin will be either serial output flag 0, based on control bit OF0 in CRB, or a receive shift register clock output.
When configured as an input, this pin may be used either as serial input flag 0, which will control status bit IF0 in the SSISR, or as a receive shift register clock input.

When this pin is configured as a transmit data pin, its direction is always output regardless of SCD0 bit value, and is fully synchronized with the other transmit data pins (STD and SC1).

SC0 may be programmed as a general-purpose I/O pin (PC0) when the ESSI SC0 function is not being used.

NOTE : The ESSI can operate with more than one active transmitter only in synchronous mode.

Serial Control 1 pin (SC1)

The function of this pin is determined by the selection of either synchronous or asynchronous mode.
For asynchronous mode (such as a single codec with asynchronous transmit and receive), this pin is the receiver frame sync I/O.
For synchronous mode, this pin is used for transmitter data out pin of transmit shift register number 2 or for drive enable tranmitter #0 signal or for serial flag SC1 and operates like the previously described SC0.
SC0 and SC1 are independent serial I/O flags but may be used together for multiple serial device selection. SC0 and SC1 can be used unencoded to select up to two codecs or may be decoded externally to select up to four codecs.
If this pin is configured as serial flag pin, its direction is determined by the SCD1 bit in the CRB.

When configured as an output, this pin will be either a serial output flag, based on control bit OF1, the transmitter#0 drive enable signal or it will make the receive frame sync signal available.
When configured as an input, this pin may be used as a serial input flag, which will control status bit IF1 in the ESSI status register, or as a receive frame sync from an external source.

When this poin is co,nfigured as a transmit data pin, its direction is always output regardless of SCD1 bit value, and is fully synchronized with the other transmit data pins (STD and SC0).

SC1 may be programmed as a general-purpose I/O pin (PC1) when the ESSI SC1 function is not being used.

NOTE : The ESSI can operate with more than one active transmitter only in synchronous mode

Serial Control 2 pin (SC2 – LRCK)

This pin is used for frame sync I/O.
SC2 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode.
The direction of this pin is determined by the SCD2 bit in CRB.
When configured as an output, this pin is the internally generated frame sync signal.
When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).

SC2 may be programmed as a general-purpose I/O pin (PC2) when the ESSI SC2 function is not being used.

2.2- Serial Communication Interface (SCI)

The SCI provides a full-duplex port for serial communication to other DSPs, microprocessors, or peripherals such as modems. The communication can be TTL-level signals or, with additional external logic, **RS232, RS422, RS485**, etc.

This interface uses three dedicated pins : transmit data (TXD), receive data (RXD), and serial clock (SCLK).
It supports **industry-standard asynchronous** bit rates and protocols as well as **high-speed synchronous** data transmission (up to **12.5 Mbit/s** for a 100 MHz clock). The asynchronous protocols include a multidrop mode for master/slave operation with **Wakeup On Idle Line and wakeup On Bit capability**.

The SCI consists of separate transmit and receive sections whose operation can be asynchronous with respect to one another. A programmable baud-rate generator provides the transmit and receive clocks. An **enable vector and an interrupt vector** have been included so that the baud-rate generator can function as a general-purpose timer when it is not being used by the SCI or when the interrupt timing is the same as that used by the SCI.

Each of the three SCI pins can be configured as either a general-purpose I/O or as a specific SCI pin. Each pin is independent of the others (e.g. if only TXD is needed, RXD and SCLK can be programmed for general-purpose I/O). However, at least one of the three pins must be selected as an SCI pin to release the SCI from reset.

SCI interrupts may be enabled by programming the SCI control registers before any of the SCI pins are programmed as SCI functions. In this case, only one transmit interrupt can be generated because the transmit data register is empty. The timer and timer interrupt will operate when one or more SCI pins is programmed as an SCI pin.

Receive Data (RXD)

This input receives byte-oriented serial data and transfers the data ot the SCI receive shift register.
Asynchronous input data is sampled on the positive edge of the receive clock (1 X SCLK) if SCKP equals zero.

RXD may be programmed as a general-purpose I/O pin (PE0) when the SCI RXD function is not being used.

Transmit Data (TXD)

This outputtransmits serial data from the SCI transmit shift register.
Data changes on the negative edge of the asynchronous transmit clock (SCLK) if SCKP equals zero. This output is stable on the positive edge of the transmit clock.

TXD may be programmed as a general-purpose I/O pin (PE1) when the SCI RXD function is not being used.

Serial Clock (SCLK)

This bidirectional pin provides an input or output clock from which the transmit and/or receive baud rate is derived in the asynchronous mode and from which data is transferred in the synchronous mode.

SCLK may be programmed as a general-purpose I/O pin (PE2) when data is being transmitted on TXD since, in the asynchronous, the clock need not be transmitted. There si no connection between programming the PE2 pin as SCLK and data coming out the TXD pin because SCLK is independent of SCI data I/O.

2.3- Timer Input Output (TIO)

The DSP56301 includes a Triple Timer Module with 3 pins TIO0, TIO1 and TIO2.
The Timer #2 is reserved for software DSP core developers and so the associated pin (TIO2) is not used on Déesse.

Timers #0, #1 and the associated pins (TIO0 and TIO1) are free for software/hardware applications.

Each timer can use internal or external clocking and can interrupt the DSP56301 after a specified number of events (clocks) or can signal an external device after counting internal events.

Each timer can also be used to trigger DMA transfers after a specified number of events (clocks) occurred.

Each timer connects to the external world through one **bidirectional pin TIO**.

When TIO is configured as input, the timer functions as an **external event counter or can measure external pulse width/signal period.**
When TIO is configured as output, the timer is functioning as either **a timer, a watchdog or a Pulse Width Modulator**.

When the TIO pin is not used by the timer it can be used as general-purpose I/O pin.

3- CODEC CONFIGURATION

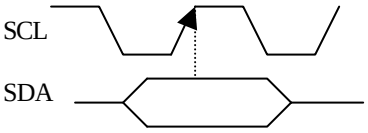
The signals SRD1, STD1, SCLK1 and LRCLK1 of the DSP ESSI#1 port are used to transfer DATA from the CODEC/DSP to the DSP/CODEC. SCLK1 & LRCLK1 are generated by the chipset to synchronize the DSP and the CODEC.

The CODEC configuration is done by a I2C channel that is realized with the SC10 and SC11 signals of the ESSI#1 port of the DSP.
SC10 pin is the I2C SCL (Serial CLock) signal and SC11 pin is the I2C SDA (Serial DAta) signal.
These two signals go to the Déesse chipset that contains a **8-bit shift serial register**.

BITS FUNCTION :

The **bits 0 to 2** encode the sampling freequency.
The **bits 3 to 5** encode the sampling resolution and the type of serial transfert.
The **bit 6** resets the CODEC.
The **bit 7** is reserved for future use/feature.

The LSB bit must be sent first. Always 8 bits must be sent because there is no way to reset the shift register, except the PCI reset from the mainboard.



To send a bit to the shift register :
1- Write 0 on the SCL line
2- Write the data value on the SDA line
3- Write 1 on the SCL line
4- Write 0 on the SCL line

Data bits (SDA) are latched on the rising edge of the clock (SCL)

3.1- Sampling Frequency : b[2,1,0]

Déesse provides 8 audio sampling rates from two master clock oscillators : 24.576 MHz and 22.5792 MHz..
The sampling rate is selected with 3 bits that are sent from the DSP to the Déesse Chipset.
The chipset is dividing the master clocks according to the bits value.

Bit code b[2,1,0]	Fs (LRCLK)	Serial Clock (SCLK)	Fs DIV	Serial DIV	Master Clock (MCLK)	External Oscillator
000	**22.05 kHz**	1.4112 MHz	256	4	5.6448 MHz	22.5792 MHz
001	24 kHz	1.536 MHz	256	4	6.144 MHz	24.576 MHz
010	**32 kHz**	2.048 MHz	384	6	12.288 MHz	24.576 MHz
011	**44.1 kHz**	2.8224 MHz	256	4	11.2896 MHz	22.5792 MHz
100	**48 kHz**	3.072 MHz	256	4	12.288 MHz	24.576 MHz
101	64 kHz	4.096 MHz	384	6	24.576 MHz	24.576 MHz
110	88.2 kHz	5.6448 MHz	256	4	22.5792 MHz	22.5792 MHz
111	**96 kHz**	6.144 MHz	256	4	24.576 MHz	24.576 MHz

Sampling frequencies of 22.05, 44.1 & 88.2 are done with a 22.5792 MHz external oscillator .
Other frequencies are done with the 24.576 MHz external oscillator.

Fs (LRCLK) = MCLK / Fs DIV
Serial Clock (SCLK) = MCLK / Serial DIV
Fs (LRCLK) = SCLK / 64 (number bits/sample)

3.2- Sampling Resolution and Serial Interface : b[5,4,3]

Déesse provides audio sampling at resolutions of 16-, 20 or 24-Bit.
The resolution is selected with 3 bits that are sent from the DSP to the Déesse Chipset.

Bit code b[5,4,3]	Resolution	Serial Interface
011	16-Bit	I2S, MSB first
100	20-Bit	I2S, MSB first
101	24-Bit	I2S, MSB first
Other	Reserved	Reserved

The DSP will always send/receive 32 bits to/from the CODEC, but only 16, 20 or 24 bits will be valid when the CODEC configuration is, respectively, 16-, 20- or 24-Bit.

The best **AUDIO Quality / DSP time** ratio is when using the CODEC in the 24-Bit format because only 8 bits are lost (not used) !
For modern AUDIO applications, it is also recommended to use 24-Bit formats.

The DSP ESSI#1 port must always be configured to use the 32-Bit MSB First I2S format :

CRA	Word Length control (WL2-WL0) Bits 21-19	= [1,0,0]	Reset value = [0,0,0]
CRB	Frame Sync Relative Timing (FSR) Bit 9	= 1	Reset value = 0

3.3- CODEC Reset and Power down : b[6]

b [6]	
0	Reset the CODEC / Power down
1	No reset / No Power down

This bit manages the CODEC's pin PDN_RSTB that has two functions : Power DowN and ReSeT (what means the 'B' ?)
The default value when power on the Déesse card (and so the computer) is 0, this means the CODEC is in a power down state. To wake up it, just turn the bit to 1.
This system allows to hold the power down pin while ramping up the power supplies (when turning ON the computer) to avoid glitches in the DAC output (remember the Falcon 030 action on your speakers !). Sure, it is strongly recommended to turn OFF the CODEC before turning OFF (standby state) the computer to avoid the same problem !

At any time, it is possible to reset the CODEC : turn the bit to 0 and turn back to 1 after a minimal delay of 10 nano seconds.

When bit 6 is returned to high, the CODEC begins a reinitialization sequence. The output data becomes valid after a minimum of 128 LRCLK cycles. During the initialization sequence, the outputs of the DAC and ADC are invalid.

Note that any change on the Sampling Resolution bits or phase shift in LRCLK triggers the reinitialization sequence.

3.4- Reserved bit : b[7]

b [7] should always be written to 0 for compatibility.

4- DSP CORE FREQUENCY

The DSP56300 core features a Phase Locked Loop (PLL) clock generator in its central processing module.
The PLL allows the processor to operate at a high internal clock frequency derived from a low-frequency clock input.

The DSP uses an input clock of 24.576 MHz.
The PLL needs an exterrnal capacitor to run correctly. The value of this capacitor was determined when designing the Déesse board regarding the frequency that may be used by the DSP.

The core frequency is calculated by the following equation :

Fcore = Fextal x MF/PDF

Where : - Fextal is the external clock input : 24.576 MHz
- MF is the Multiplication Factor : 1 to 4096 (see the 56300 Family manual)
- PDF is the Predivider : 1 to 16 (see the 56300 Family manual)

To fixe a practical value for the external capacitor, it was decided that the PDF = 3
Déeese uses a 12 nF capacitor.

Here are the following core frequencies that are supported by Déesse, depending of the MF and the DSP model :

MF value	**Core Frequency (MHz)**	
13	79.872	Not recommended with a 12 nF capacitor → change by a 10 nF
14	**86.016**	**Recommended frequency for a 80 MHz model with 12ns SRAM**
15	**92.16**	
16	**98.304**	
17	**104.448**	**Recommended frequency for a 100 MHz model**
18	**110.592**	
19	**116.736**	Heatsink is recommended for a 100 MHz model
20	122.88	Use a heatsink for a 100MHz model !
21	129.024	Use a heatsink for a 100 MHz model !

The SRAM must have a time access of **10ns for a DSP at 100 MHz** if you want access with 2cycles (the minimum).

If the core frequency is increased, according to the timing tolerance of the SRAM, the access time of the SRAM must be decreased OR **Wait States** must be programmed to slow the SRAM accesses.

END