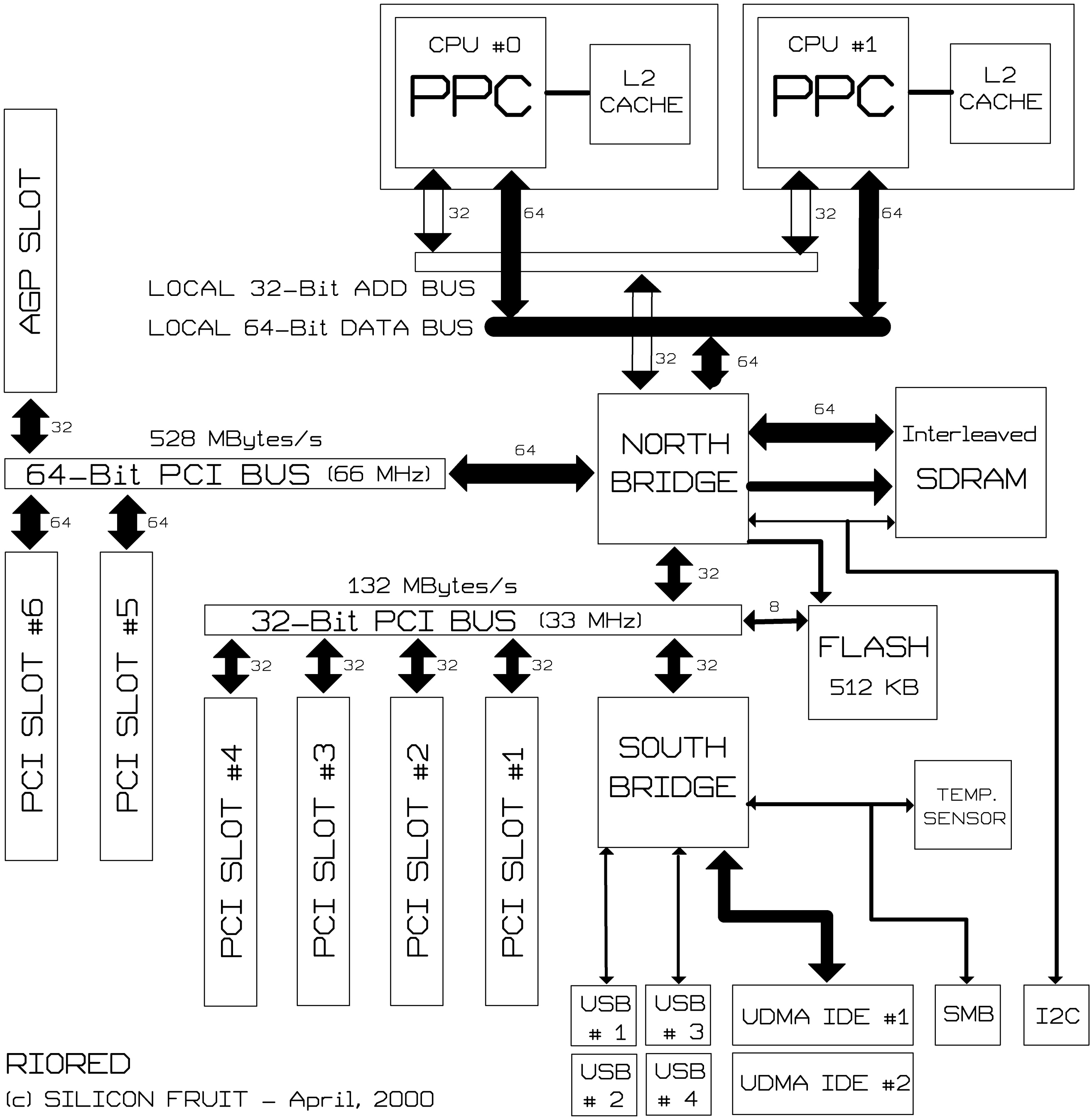
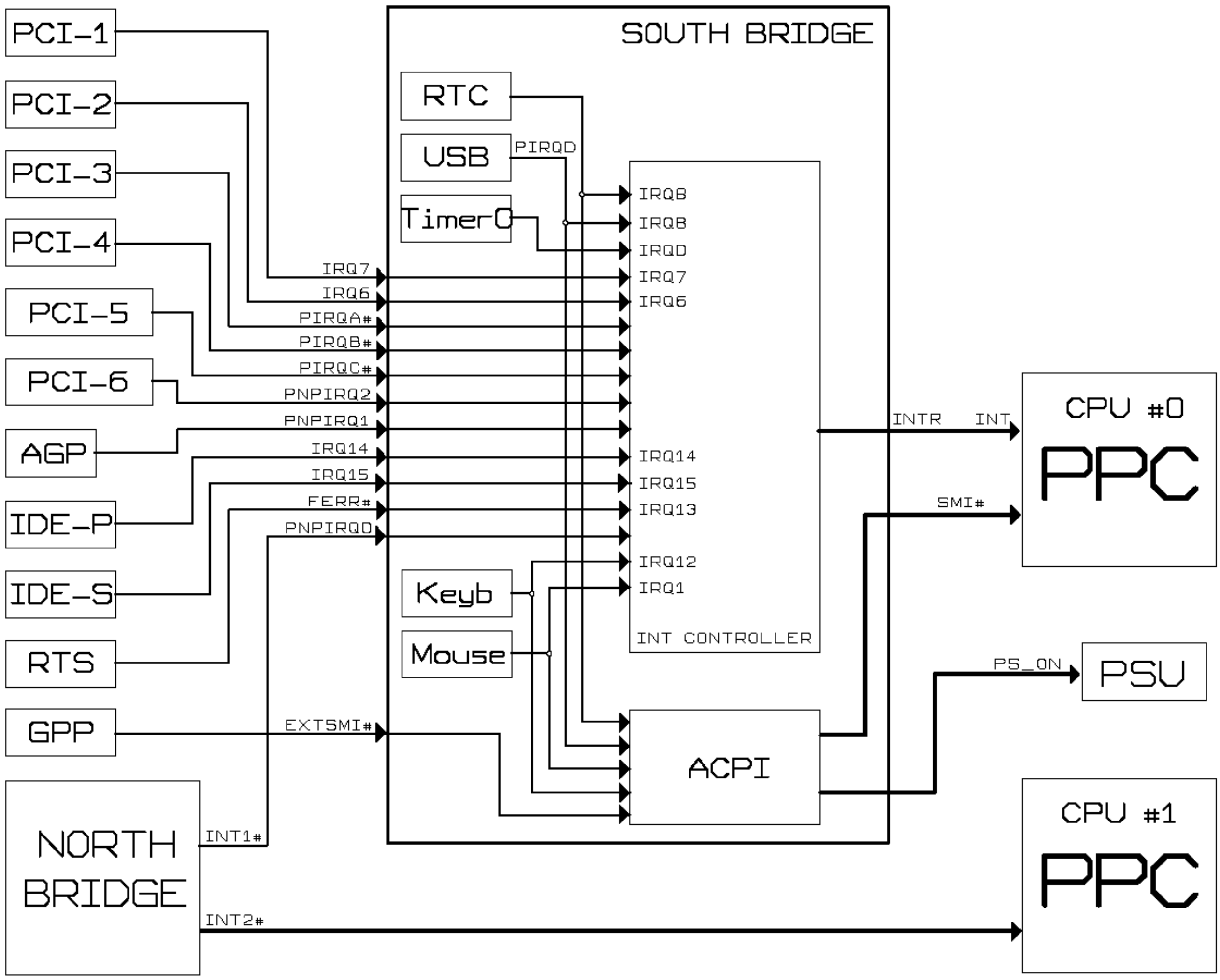
ROHB
Riored Open Hardware Book

Rev. 0.7 – September, 14th 2000 – Rodolphe Czuba : rczuba@free.fr

1- HARDWARE OVERVIEW



2- INTERRUPTS



RIORED INT MAP – Rodolphe Czuba – March 2000

All the interrupts are treated by the CPU0. The CPU1 only treats one interrupt that is generated by a register of the CPC710 and presented on the pin INT1#. It allows the CPU0 to interrupt the CPU1 in the SMP architecture. The CPU1 cannot interrupt the CPU0.

SOURCE	VIPER PIN	VIPER IRQ	ROUT STATUS	COMMENTS
Timer_0	--	0	Fixed	System Timer
PS/2_Keyboard	--	1	Fixed	
USB / RTC	--	8	Free / Fixed	USB uses PIRQD#
CPC-710 DMA	PNPIRQ0	9	Free	Should be used for AGP.
AGP	PNPIRQ1	10	Free	
PCI_6	PNPIRQ2	11	Free	PCI-64
PS/2_Mouse	--	12	Fixed	
RTS	FERR#	13	Fixed	Remote Temperature Sensor
IDE_Primary	IRQ14	14	Fixed	
IDE_Secondary	IRQ15	15	Fixed	
PCI_5	PIRQC#	3	Free	PCI-64
PCI_4	PIRQB#	4	Free	PCI-32
PCI_3	PIRQA#	5	Free	PCI-32
PCI_2	IRQ6	6	Fixed	PCI-32
PCI_1	IRQ7	7	Fixed	PCI-32

AGP & PCI6 could be exchanged with IDE_P & IDE_S, because of the choice between IRQ[14,15] and [10,11] for the IDE ports. PNPIRQ[x] and IRQ[6,7] are logically inversed with a 74LVC04 circuit on the main board.

4- SLOT-P : The PPC Processor Slot

There are two processor slots on RIORED to allow a **SMP architecture with two identical processors**.
The RIORED processor slot uses a SC242 connector (SLOT 1) and is called **SLOT-P.**

It is assumed that the reader is familiar with the 60x and MPX signals. For further information, please refer to the BUS INTERFACE MANUAL (MPCBUSIF/AD), the USER'S MANUAL (chapter 7) and the HARDWARE SPECIFICATION MANUAL of the apropriate processor.

A- 60x and MPX Bus Protocol Support

The **SLOT-P** supports the **60x bus protocol** and the new **MPX bus protocol** first provided on MPC7400 (**G4)** processor.

MPX bus protocol is a enhanced 60x bus protocol that is selectable by the pin EMODE# on the G4.

The signals used for the 60x and MPX bus protocols are largely identical, except that the MPX bus mode doesn't use the ABB# and DBB# outputs (I/O on 60x & 7xx CPU), replaces the DBWO# input with the DTI[0:2] inputs, replaces the SHD# signal with SHD[0:1]# and adds the HIT# and DRDY# signals.
For this reason, like with the G4 pinout, some pins of the SLOT-P have two names separated by '-' : the first name is for the 60x bus and the second name is for the MPX bus.
Some pins/signals are only provided for the MPX protocol and are so mentioned 'MPX'.
Pins/signals that are only used with 60x Bus Protocol are mentioned '60x'.

B- SLOT-P Functional Groupings

'#' signifies the signal is active at the low level

Address Arbitration	BR#, BG#, ABB#(60x)
Address Bus	A[0:31], AP[0:3], ARes[0:3]
Address Transfer Attributes	TS#, TT[0:4], TBST#, TSIZ[0:2], GBL#, WT#, CI#
Address Termination	AACK#, ARTRY#, SHD#-SHD0#(MPX), SHD1#(MPX), HIT#(MPX)
Data Arbitration	DBG#, DBB#(60x), DBWO#-DTI0(MPX), DTI1(MPX), DTI2(MPX), DRDY#(MPX)
Data Transfer	DH[0:31], DL[0:31] (D[32:63]), DP[0:7]
Data Termination	TA#, TEA#
Interrupts & Reset	INT#, SMI#, MCP#, CKSTP_IN#, CKSTP_OUT#, SRESET#, HRESET#
Processor Status & Control	RSRV#, TBEN, QREQ#, QACK#, EMODE#
Clock Control	SYSCLK
Test Interface (JTAG/COP)	TRST#, TMS, TCLK, TDI, TDO
Security	INTRUDER#, NC[0:4]
Power Supplies	VCC_CORE (16), CORE_VID (5), VCC_BUS (9), VCC_3.3 (4), VCC_5 (1), VCC_12 (1) The SC242 connector allows up to 1 Ampere per pin.
Grounds	GND (36)
Reserved	Reserved (6)

C- SLOT-P signals not used by RIORED R.1

The following signals are not used by RIORED R.1

ABB#, DBB#, WT#, CI#, DBWO#, CKSTP_OUT#, RSRV#, QREQ#, QACK#, EMODE#
SHD1#(MPX), HIT#(MPX), DTI1(MPX), DTI2(MPX), DRDY#(MPX)

D- x86 SLOT 1 and Riored SLOT-P confusion

Two SC242 (commonly called SLOT1) connectors are used, but sure the pinout is not the same than the one of the Pentium II/III & CELERON SLOT1.

A particular attention was taken when designing the pinout of the SLOT-P to avoid some dramatical accidents when users may attempt to plug a P2/P3 daughter board on RIORED or, in the reverse way, to plug a PPC daughter card in the SLOT1 of a x86 main board…

If a x86 daughter card is plugged in the SLOT-P a signal (INTRUDER#) will keep the Riored power supply to turn on. Riored's electronic is so secured and the 'indruder' card too !

In the reverse way, if the user attempts to plug a PPC daughter card in the SLOT1 of a x86 PC main board, the VID[0:4] pins of the SLOT1 (called NC[0:4] on SLOT-P) will stay not connected (open) because of the fact that the NCx (Not Connected) pins on the PPC daughter card must never be connected.
In this manner, the Voltage Switching Regulator of the x86 main board will be turned OFF (VID[0:4]=11111) and the PPC card is secured.

Keep in mind that plugging a x86 card in the SLOT-P or plugging a PPC card in the SLOT1 stills to be a big mistake that is DANGEROUS for your hardware ! But a such problem already exists in the x86 PC world with cards like ATHLON that use a SC242 connector with a different pinout than on SLOT1, called SLOT A…

E- Other signals of the SLOT-P

- A **VCC_12** is provided to power a fan. The wires of the fan may be soldered on two dedicated pads, avoiding to use a fan connector on the main board.

- The four pins **ARes[0:3]** are reserved for the future 36-Bit Address (64GB memory range) bus provided on future PPC processors like the G4+.

- The **INTRUDER#** pin is the same pin number than the SLOTOCC# pin of the SLOT1.
  This pin is always connected to ground on the P2/3 & Celeron daughter cards and must never be connected on a PPC daughter cards. See above sub-chapter (D) for the function of this pin.

- The pins **NC[0:4]** are the same pin numbers than the VID[0:4] pins of the SLOT1.
  These pins give the indication of the core voltage level on a x86 daughter card.
  They must never be connected on a PPC daughter card. See above sub-chapter (D) for the function of this pin.

F- 60x BUS signals not implemented on the SLOT-P and CPC-710

Only present on 601, 603 & 604 processors :	XATS#, APE#, DPE#, TCn#, CSEn
Only present on 601 processor :	QUIESC_REQ, SYS_QUIESC#, RESUME
Only present on 604 processor :	HALTED, RUN
Not present on G4 / Not recommended :	TLBISYNC#, DBDIS#, DRTRY#

601 and 604 Processors are now end-of-life.
Use of the DBDIS# and DRTRY# signals is not recommended for new designs.
DRTRY# must be grounded to select the no-DRTRY mode of the CPU.

SLOT-P PINOUT

SIGNAL NAME	PIN (L)	PIN (R)	SIGNAL NAME
VCC_12	**A001**	**B001**	**GND**
GND	**A002**	**B002**	**VCC_CORE**
INT0#	A003	**B003**	**VCC_CORE**
SMI#	A004	B004	CORE_VID0
EMODE#	A005	B005	CORE_VID1
GND	**A006**	B006	CORE_VID2
QACK#	A007	**B007**	**VCC_CORE**
QREQ#		A008	**B008 VCC_CORE**
RSRV#	A009	B009	CORE_VID3
GND	**A010**	B010	CORE_VID4
SYSCLK	A011	B011	*WT#*
SHD#-SHD0#	A012	**B012**	**VCC_CORE**
SHD1#	A013	**B013**	**VCC_CORE**
BSEL1	A014	B014	*CI#*
DBWO#-DTI0	A015	B015	*DTI1*
DTI2	A016	B016	*DRDY#*
A31	A017	**B017**	**VCC_CORE**
GND	**A018**	**B018**	**VCC_CORE**
A30	A019	B019	A29
A28	A020	B020	Reserved
A27	A021	B021	A26
GND	**A022**	B022	A25
A24	A023	B023	A23
A22	A024	B024	A21
A20	A025	**B025**	**VCC_CORE**
GND	**A026**	B026	A19
A18	A027	B027	A17
A16	A028	B028	A15
A14	A029	**B029**	**VCC_CORE**
GND	**A030**	B030	A13
A12	A031	B031	A11
A10	A032	B032	A9
A8	A033	**B033**	**VCC_CORE**
GND	**A034**	B034	A7
A6	A035	B035	A5
A4	A036	B036	A3
A2	A037	**B037**	**VCC_CORE**
GND	**A038**	B038	A1
A0	A039	B039	*ARes3*
ARes2	A040	B040	*ARes1*
ARes0	A041	**B041**	**GND**
GND	**A042**	B042	AP0
AP1	A043	B043	AP2
AP3	A044	B044	GBL#
TBEN	A045	**B045**	**VCC_CORE**
GND	**A046**	B046	TS#
TA#	A047	B047	BR#
ARTRY#	A048	B048	DBG#
TEA#	A049	**B049**	**VCC_CORE**
GND	**A050**	B050	BG#
AACK#	A051	B051	*ABB#*
DBB#	A052	B052	DL0
DL1	A053	**B053**	**VCC_CORE**
GND	**A054**	B054	DL2
DL3	A055	B055	DL4
DL5	A056	B056	DL6
DL7	A057	**B057**	**VCC_CORE**
GND	**A058**	B058	DL8
DL9	A059	B059	DL10
DL11	A060	B060	DL12
DL13	A061	**B061**	**GND**

SIGNAL NAME	PIN (L)	PIN (R)	SIGNAL NAME
GND	**A062**	B062	DL14
DL15	A063	B063	DL16
DL17	A064	B064	DL18
DL19	A065	**B065**	**VCC_BUS**
GND	**A066**	B066	DL20
DL21	A067	B067	DL22
DL23	A068	B068	DL24
DL25	A069	**B069**	**VCC_BUS**
GND	**A070**	B070	DL26
DL27	A071	B071	DL28
DL29	A072	B072	DL30
DL31	A073	**B073**	**VCC_BUS**
GND	**A074**	B074	DH0
DH1	A075	B075	DH2
DH3	A076	B076	DH4
DH5	A077	**B077**	**VCC_BUS**
GND	**A078**	B078	DH6
DH7	A079	B079	DH8
DH9	A080	B080	DH10
DH11	A081	**B081**	**GND**
GND	**A082**	B082	DH12
DH13	A083	B083	DH14
DH15	A084	B084	DH16
DH17	A085	**B085**	**VCC_BUS**
GND	**A086**	B086	DH18
DH19	A087	B087	DH20
DH21	A088	B088	DH22
DH23	A089	**B089**	**VCC_BUS**
GND	**A090**	B090	DH24
DH25	A091	B091	DH26
DH27	A092	B092	DH28
DH29	A093	**B093**	**VCC_BUS**
GND	**A094**	B094	DH30
DH31	A095	B095	DP0
DP1	A096	B096	DP2
DP3	A097	**B097**	**VCC_BUS**
GND	**A098**	B098	DP4
DP5	A099	B099	DP6
DP7	A100	**B100**	**GND**
TBST#	A101	B101	*INTRUDER#*
GND	**A102**	B102	TSIZ0
TSIZ1	A103	B103	TSIZ2
TT0	A104	B104	TT1
TT2	A105	**B105**	**VCC_BUS**
GND	**A106**	B106	TT3
TT4	A107	B107	MCP#
CKSTP_IN#	A108	B108	*CKSTP_OUT#*
SRESET#	A109	**B109**	**VCC_5**
GND	**A110**	B110	HRESET#
Reserved	A111	B111	*Reserved*
Reserved	A112	B112	*Reserved*
Reserved	A113	**B113**	**VCC_3.3**
GND	**A114**	B114	*TDI*
TRST#	A115	B115	*TDO*
VCC_3.3	**A116**	B116	*TCK*
Reserved	A117	**B117**	**VCC_3.3**
GND	**A118**	B118	*TMS*
NC0	A119	B119	*NC1*
NC2	A020	B120	*NC3*
NC4	A121	**B121**	**VCC_3.3**

5- GPP : Geek & Panel Port

Riored mainboard provides the standard connects to the front panel of the case you use, but it provides too a amazing ‘GEEK’ port from a SMBus (that is I2C compatible), and a LCD DISPLAY connector, an other amazing feature of Riored.

Onto the mainboard there are two features that are managed by the I2C and the SMBus. Respectively, they are DIMM Identification (DIMM Id) and the Remote Temperature Sense (RTS).

A- Pinout

The LCD (I2C), the SMBus and the Front Panel signals are grouped on a common connector that is a standart 2 Rows HE13 Male connector with a total of 26 pins (2x13). This last can be prolongated by a standard (DB25 connector + 26 wires ribbon cable) backpanel metal bracket, if needed.
The GPP is near the edge of the board.

POWER LED +	**1**	**14**	**SPEAKER +**	
NC	**2**	**15**	**NC**	**FRONT PANEL**
POWER LED -	**3**	**16**	**NC**	
HDD LED +	4	**17**	**SPEAKER -**	
HDD LED –	5	18	I2C +5V	
POWER SW	**6**	19	I2C SCL	
POWER SW GND	**7**	20	I2C SDA	**LCD**
RESET SW	8	21	I2C GND	
RESET SW GND	9	22	*Reserved*	
SMBus +5V	**10**	**23**	**+3.3V**	
SMBus CLK	**11**	**24**	**+5VSB**	**GEEK**
SMBus DATA	**12**	**25**	**EXTSMI#**	
SMBus GND	**13**	**26**	*Reserved*	

B- SMBus

The SMBus is provided by the VIPER South Bridge and is used by the RTS (Remote Temperature Sensor) chip and the GPP connector.
This last one gives to geek users the possibility to connect their own small electronic module using the pin 10 to 13 and optionally the pin 23 to 25 that provide +3.3V, +5VSB (standby power supply) and an interrupt signal that is able to wake up the system (going from ‘standby’ mode to ‘full’ mode). The geek module should use a HE13/14 Femal connector with one or two rows of four pins.

6- RTS : Remote Temperature Sensor

Riored is equiped with a numerical temperature sensor, the MAX 1669, which monitors the temperature of a PN junction (transistor) placed on the board. The MAX1669 monitors too the temperature of its own body.

This chip sends an IRQ13 to the VIPER if the temperature is too low or too high on one of the two captors.
More, the MAX 1669 controls the fan that is present on each CPU. The two fans are managed together.

All RTS registers are accessible by software via the SM Bus of the VIPER.

The task of the software is to initialize and read the mini and maxi temperatures of the RTS, and to select the appropriate speed of the fans.

The software must so wait for a thermical interrupt provided by the CPU die or by the RTS, and it must act on the fan speed and, eventually, reduce the clock of the CPU(s) during a moment…

7- FTP : Flash Transfert Port

RioRed is furnished with a special port to allow you to transfert, from the parallel port of a computer, a new software code into the flash. It is a necessity when debugging a new BIOS code by example.

This port uses a handshaking that is a subset of the one of the known ECP port you can find in all modern computers. The transfer rate is from 500 to 1000 KBytes/s, depending of the software and the hardware at each side.
The FTP port uses a standart HE13 male 2x13 pin connector that has to be prolongated by a standard (DB25 connector + 26 wires ribbon cable) backpanel metal bracket.

In the following explanations, the 'HOST' term describes the PC (Personal Computer) you use to send the code in the Riored flash, and the term 'PERIPH' describes the Riored motherboard.

The link between the HOST and the PERIPH must be done by a standart ECP cable or a cable that uses a minimal connection as described below.

For the standart port, the signal names are doubled : the first is the SPP (Standart Parallel Port) name and the second is the ECP (Extended Capabilities Parallel Port).

A- SPP/ECP standart connector (backpanel Female DB25)

Bold signal are used by FTP handshaking

SPP	ECP	IO	SPP	ECP	IO
1 Strobe#	**HostCLK**	**Out**	14 Autofeed#	HostACK	Out
2 Data 0	**Data 0**	**I/O**	15 Fault#	PeriphREQ	In
3 Data 1	**Data 1**	**I/O**	**16 Init#**	**ReversREQ#**	**Out**
4 Data 2	**Data 2**	**I/O**	**17 Select_In#**	**1284 Active**	**Out**
5 Data 3	**Data 3**	**I/O**	**18 Gnd**		
6 Data 4	**Data 4**	**I/O**	**19 Gnd**		
7 Data 5	**Data 5**	**I/O**	**20 Gnd**		
8 Data 6	**Data 6**	**I/O**	**21 Gnd**		
9 Data 7	**Data 7**	**I/O**	**22 Gnd**		
10 /Ack	**PeriphCLK**	**In**	**23 Gnd**		
11 Busy	PeriphACK	In	**24 Gnd**		
12 PError	ACKReverse#	In	**25 Gnd**		
13 Select	X-flag	In			

B- RIORED FTP connector - Backpanel Female DB25

1	**HostCLK**	**Out**	14	nc
2	**Data 0**	**I/O**	15	nc
3	**Data 1**	**I/O**	16	nc
4	**Data 2**	**I/O**	17	nc
5	**Data 3**	**I/O**	**18**	**Gnd**
6	**Data 4**	**I/O**	**19**	**Gnd**
7	**Data 5**	**I/O**	**20**	**Gnd**
8	**Data 6**	**I/O**	**21**	**Gnd**
9	**Data 7**	**I/O**	**22**	**Gnd**
10	**PeriphCLK**	**In**	**23**	**Gnd**
11	nc		**24**	**Gnd**
12	**ACKReverse#**	**In**	**25**	**Gnd**
13	**FTP Active**	**In**		

C- RIORED FTP connector – HE13 Male 2x13 pins on the motherboard.

1	**HostCLK**	**Out**	14	nc
2	**Data 0**	**I/O**	15	nc
3	**Data 1**	**I/O**	16	nc
4	**Data 2**	**I/O**	17	nc
5	**Data 3**	**I/O**	**18**	**Gnd**
6	**Data 4**	**I/O**	**19**	**Gnd**
7	**Data 5**	**I/O**	**20**	**Gnd**
8	**Data 6**	**I/O**	**21**	**Gnd**
9	**Data 7**	**I/O**	**22**	**Gnd**
10	**PeriphCLK**	**In**	**23**	**Gnd**
11	nc		**24**	**Gnd**
12	**ACKReverse#**	**In**	**25**	**Gnd**
13	**FTP Active**	**In**	26	nc

D- LINK CABLE

You have to use a ECP cable or to construct yourself your cable by connecting the following pins of two Male DB25 connectors :

Host	Riored	
1 -----	10	Host to Periph CLK
2 -----	2	Data 0
3 -----	3	Data 1
4 -----	4	Data 2
5 -----	5	Data 3
6 -----	6	Data 4
7 -----	7	Data 5
8 -----	8	Data 6
9 -----	9	Data 7
10 -----	1	Periph to Host CLK
16 -----	12	Host to Periph Reverse signal (Req / Ack)
17 -----	13	FTP active signal from Host
18 -----	**18**	**GND**
19 -----	**19**	**GND**
20 -----	**20**	**GND** **To ensure good transferts,**
21 -----	**21**	**GND** **it is important to connect all the Ground (pin 18 to 25) wires !**
22 -----	**22**	**GND** **Use of a Ground Shielded cable is recommended.**
23 -----	**23**	**GND** **The lengh of the cable should be reasonable : 2 meters**
24 -----	**24**	**GND**
25 -----	**25**	**GND**

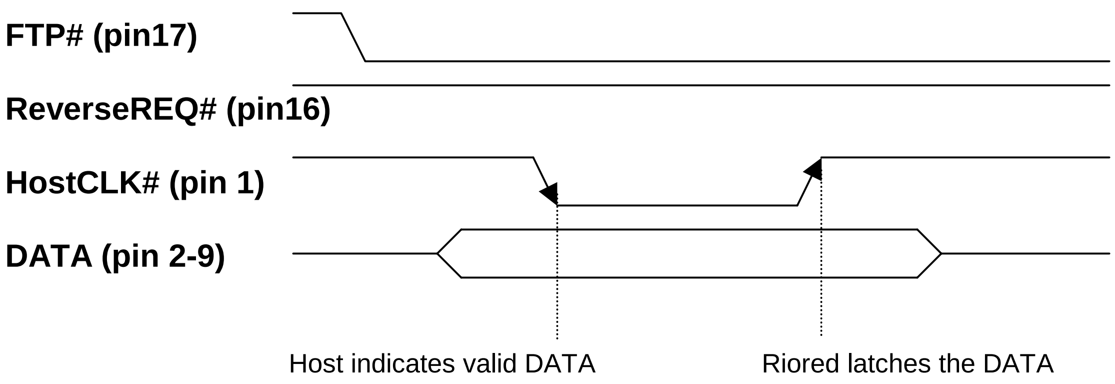
Warning : a such minimal cable is not symetrical ! The left connector must be connected to the HOST and the right connector must be connected to Riored. To avoid this problem you have to add the connections 12 to 16 and 13 to 17 (left to right order).

E- FTP CYCLES

The FTP handshaking uses a subset of the ECP handshaking.
Like with ECP, the HostCLK is used, but the PeriphACK is not used to confirm the transfert.

There is 2 cycles that must be distinguished : Forward (Write) and Reverse (Read).
Forward cycle is used to send ADDresses to the flash (Write and Read cycles) and to send DATA for write cycles.
Reverse cycle is used only to receive from Riored the DATA from the Flash in a Read cycle (i.e. the second step of the Flash 'Program & verify' command).

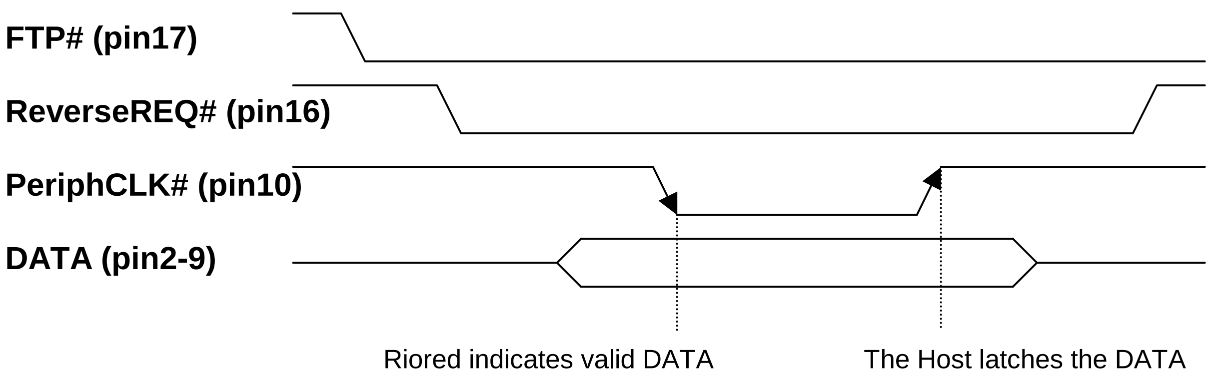
Figure of the FTP Forward Cycle (Write) – 1 byte



Steps :

1- Data is placed on data lines (D0-D7) by Host.
2- Host indicates valid data by asserting HostCLK# low (pin 1 on the HOST).
3- Host de-asserts HostCLK# high. Positive edge is used by Riored to shift data.
4- Data is removed of data lines by Host.

Figure of the FTP Reverse Cycle (Read) – 1 byte



Steps :

1- Host asserts ReverseREQ# to indicate a reverse (read) cycle.
2- Assuming the address has already been sent with write cycles, Riored places the data on data lines.
3- Riored (Periph) indicates valid data by asserting PeriphCLK# low.
4- Riored de-asserts PeriphCLK# high. Positive edge is used by Host to shift data.
5- Host de-asserts ReverseREQ# to end the reverse cycle.
6- Data is removed of data lines by Riored.
7- Host de-asserts ReverseREQ# to return to the Forward mode (write).

8- DC-DC VOLTAGE REGULATORS

RIORED has two DC-DC switching regulators, VR1 and VR2.
The Evaluation board (R.1) don't need a second regulator (VR2)

VR1furnishes the CPU CORE voltage from 1.3 to 3.5 V with current up to 35A. It is selectable with 5 CORE_VID pins on the –SLOT-P. VR2, not needed on Riored R.1, furnishes a fixed 2.5V, that may evoluate to 1.8V on future Riored 2 model.

CPU VOLTAGE (VR1) IDENTIFICATION CODE 0 = connected to GND / 1 = open

VID4	VID3	VID2	VID1	VID0	VCC_CORE	VID4	VID3	VID2	VID1	VID0	VCC_CORE
0	1	1	1	1	1.30 V	**1**	**1**	**1**	**1**	**1**	**0 V (no CPU)**
0	1	1	1	0	1.35 V	**1**	**1**	**1**	**1**	**0**	**2.1 V**
0	1	1	0	1	1.40 V	1	1	1	0	1	2.2 V
0	1	1	0	0	1.45 V	1	1	1	0	0	2.3 V
0	1	0	1	1	1.50 V	1	1	0	1	1	2.4 V
0	1	0	1	0	1.55 V	**1**	**1**	**0**	**1**	**0**	**2.5 V**
0	1	0	0	1	1.60 V	1	1	0	0	1	2.6 V
0	1	0	0	0	1.65 V	1	1	0	0	0	2.7 V
0	0	1	1	1	1.70 V	1	0	1	1	1	2.8 V
0	0	1	1	0	1.75 V	1	0	1	1	0	2.9 V
0	**0**	**1**	**0**	**1**	**1.80 V**	1	0	1	0	1	3.0 V
0	0	1	0	0	1.85 V	1	0	1	0	0	3.1 V
0	0	0	1	1	1.90 V	1	0	0	1	1	3.2 V
0	0	0	1	0	1.95 V	**1**	**0**	**0**	**1**	**0**	**3.3 V**
0	**0**	**0**	**0**	**1**	**2.00 V**	1	0	0	0	1	3.4 V
0	**0**	**0**	**0**	**0**	**2.05 V**	1	0	0	0	0	3.5 V

1- RIORED 1 CPC710-100 + IBM PPC750cx (on-chip L2 Cache)

	Source	Voltage
CPU CORE	VR1	1.8V
CPU BUS	VR2	2.5V

2- RIORED 1 CPC710-100 + IBM PPC750cx (on-chip L2 Cache)

	Source	Voltage
CPU CORE	VR1	1.8V
CPU BUS	VR2	2.5V

3- RIORED 2 QUASAR II + IBM PPC750cx/cxe (on-chip L2 Cache)

	Source	Voltage
CPU CORE	VR1	1.8V
CPU BUS	VR2	2.5V

9- PARTS REFERENCES

PROCESSORS

PRODUCER	PRODUCT	ORDERING REF.	SPEED	COMMENTS
IBM	PPC750L	IBM25PPC750L-GB500A2T	300-500	Pid8p **copper** mask
MOTOROLA	MPC750P G3	XPC750PRX400RE	366-450	P release : 2.05V core
MOTOROLA	MPC7400 G4	XPC7400RX--- ??	300-450	1.8-2.1V core ?
	MPC7400 G4	XSC7400RX400PE	400	2.15V core
	MPC7400 G4	XSC7400RX400NG	400	2.10V core

L2 CACHE MEMORIES

PRODUCER	PRODUCT	ORDERING REF.	SPEED	COMMENTS
IBM	L2 128Kx36	IBM043641WLAD	3.3/3.7/4/5/7	Late Write – BGA – 3.3/3.3-2.5
IBM	L2 **256K**x36	IBM0436A86SQKA		Pip. Burst R/R – 3.3/3.3
IBM	L2 **256K**x36	IBM0436A81DLAB		Pip. Burst R/R with self LATE - 3.3/1.9
IBM	L2 128Kx36	IBM0436A41DLAB		Pip. Burst R/R with self LATE - 3.3/1.9
MOTOROLA	L2 **256K**x36	MCM63R836A	2.7/3/3.3/3.7/4	Late Write R/R- FC-BGA – 3.3/HSTL
MOTOROLA	L2 128Kx36	MCM63R736	3/3.3/3.7/4	Late Write R/R- FC-BGA – 3.3/HSTL
MOTOROLA	L2 **256K**x36	MCM63P837	225/200/166	Pip. Burst R/R- TQFP/PBGA – 3.3/3.3-2.5
MOTOROLA	L2 128Kx36	MCM65P737	250/225/200	Pip. Burst R/R- TQFP/PBGA – 3.3-1.8/1.8
MOTOROLA	L2 128Kx**32**	MCM65P733	250/225/200	Pip. Burst R/R- TQFP – 1.8/1.8
MOTOROLA	L2 128Kx**32**	MCM63P733B	250/225/200	Pip. Burst R/R- TQFP – 3.3/3.3-2.5

VOLTAGE REGULATORS

PRODUCER	PRODUCT	ORDERING REF.	COMMENTS		
MAXIM	MAX1638	MAX1638	5-Bit VID/35A	3.85$/1K	
NATIONAL	LM2636	LM2636	5-Bit VID/20A	1.60$/1K	tube of 36
NATIONAL	LM2637	LM2637M	5-Bit VID/20A+2 linears	2.10$/1K	tube of 36

POWER ATX CONNECTOR

PRODUCER	PRODUCT	ORDERING REF.	COMMENTS
MOLEX	MB conn.	39-29-9202	See w/ or w/o pigs

USB CONNECTOR

PRODUCER	PRODUCT	ORDERING REF.	COMMENTS
MOLEX	Double Stack	87525-0001	

DIMM CONNECTOR

PRODUCER	PRODUCT	ORDERING REF.	COMMENTS
MOLEX	DIMM168	71251-0012	Plastic pegs / 2.59$ -
MOLEX	DIMM168	71736-0011	Metal pegs
AMP	DIMM168	179711-2	
FCI	DIMM168	91145-60002	Platique pegs / Noir
FCI	DIMM168	91145-61002	Metal pegs / Noir
FCI	DIMM168	91145-61022	Metal pegs / Ivoire

LITHIUM BATTERY & HOLDER

PRODUCER	PRODUCT	ORDERING REF.	COMMENTS
SONY ?	HOLDER	HL25-F/P	
---	BATTERY	CR2025	

CLOCK DRIVERS / GENERATORS

PRODUCER	PRODUCT	ORDERING REF.	COMMENTS
TI	CDC924	CDC924DL	SSOP 56
TI	CDC2509B	CDC2509BPW	TSSOP 24

LOGIC

PRODUCER	PRODUCT	ORDERING REF.	COMMENTS
TI	ALVCH162268	74ALVCH162268DL	SSOP 56
TI	AHCT04	74AHCT04D	SO 14
TI	AHCT1G04	74AHCT1G04DBV	SOT-23 5 pins
TI	AHCT1G32	74AHCT1G32DBV	SOT-23 5 pins

SOCKET 7 (321 pins)

PRODUCER	PRODUCT	ORDERING REF.	COMMENTS
AMP	Socket 7	916715-1/2/3	